Realize Your Product Promise™



Slwave Training Signal and power Integrity analysis for complex PCBs and IC packages

Fluid Dynamics

Structural Mechanics

Electromagnetics

Systems and Multiphysics

ANSYS EBU Vision: Electronic Systems





ANSYS Electronic Business Unit Driving Chip-Package-System Convergence



ANSYS High Speed Digital Design Issues









Functionality	Slwave – DC	Slwave – Pl	Slwave
ECAD Translation	\checkmark	✓	\checkmark
SIwave & 3D Layout GUI	\checkmark	✓	\checkmark
I ² R DC solver	\checkmark	✓	\checkmark
DC Path Resistance Solver	\checkmark	✓	\checkmark
Leadframe Editor 🚽 e w	\checkmark	✓	\checkmark
Plane Resonance Solver		✓	\checkmark
Automated Decoupling Analysis Optimization		✓	\checkmark
SYZ Solver		✓	\checkmark
Frequency Sweep Solver		✓	\checkmark
Synopsys HSPICE Integration		✓	\checkmark
AEDT Integration AC SYZ Solver Integration	e w	✓	\checkmark
Zo & Crosstalk Scanner N e w			\checkmark
TDR Wizard			\checkmark
Near-Field solver			\checkmark
Far-Field Solver			\checkmark
Signal Net Analyzer			\checkmark
Circuit Analysis (IBIS, IBIS-AMI, QE, VE,)	1		\checkmark
PSPICE syntax model support in Nexxim	X		\checkmark



ANSYS What is ALinks for EDA [™]?

• Integrate Electrical CAD (ECAD) to ANSYS Software



- ANSYS ALinks for EDA (once called AnsoftLinks for ECAD) streamlines the transfer of design databases from popular third-party EDA layout tools into ANSYS electromagnetic, thermal and mechanical simulation products. EDA links are available for a number of tools offered by Altium, Cadence, Mentor Graphics, Sigrity and Zuken.
- This license give you access to an **ANSYS menu in your layout tool** (after installing ECADtranslator) and to the **Slwave GUI** to prepare your simulation project.
- Translator / Editor / Link from a 3rd party layout tool to ANSYS Solvers





Allegro

APD

Supported ECAD Translations

Cadence

٠

⇒	16.0. 16.1. 16.2. 16.3. 16.5. & 16.6
-	1010, 1011, 1012, 1013, 1013, 0 1010

- 16.0, 16.1, 16.2, 16.3, 16.5, & 16.6 ⇒
 - 16.0, 16.1, 16.2, 16.3, 16.5, & 16.6 ⇒
 - 5.10, 6.14, 6.15, & 6.16 (Linux only) ⇒

Mentor Graphics

Virtuoso

SiP Digital/RF

Expedition

- **Boardstation**
- **Boardstation XE**
- PADS

Zuken (Sold by Zuken)

- **CR5000**
- **CR8000**

ODB++

- **Altium Designer**
- **Mentor Expedition** •
- Mentor PADS
- **Zuken Cadstar** .

IPC-2581

- Pulsonix
- Altium Designer (BETA) .

Other ECAD Formats

- .anf
- .gds
- .xfl
- .dxf

- **ANSYS** neutral file format ⇒
- **IC Chip format** ⇒
- **Apache Sentinel format** ⇒
- AutoCad drawing format ⇒

Added Lead Frame Editor capability to Slwave and ANSYS Electronics Desktop

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⇒	v2005, v2007.1 thru EE7.9 (uses HKP design flow)	

- ⇒ 8.x (uses HKP design flow)
 - v2007, v2007.1, v2007.2, v2007.3 and v2007.7 (uses HKP design flow) ⇒
 - PowerPCB v5.2a, v2005 and v2007 (ASCII Flow) ⇒

10 and higher (Zuken translator for .anf & .cmp) ⇒

- 2013 and higher (Zuken translator for .anf & .cmp) ⇒
- **R10 and greater** ⇒
- EE7.9.1 and greater ⇒
- 9.4 and greater ⇒
- 12.1 and greater ⇒
 - Revision 8.5 build 5905 and greater
- v2015 and greater

- ⇒
- ⇒

Realize Your Product Promise™



Design Automation for Layout



Structural Mechanics

Electromagnetics

Systems and Multiphysics

ANSYS Software Installation

- Software needed for this training class
 - ECADtranslator (for file translation), Slwave and ANSYS License Manager
 - A user is able to download all of the above software from ANSYS Customer Portal. Click on Download > Current Releases (17.x) and then choose "ANSYS Electromagnetics products" to select the above products.

ANSYS License Manager installation

- ANSYS License Manager package on **Tools** section
- Specify license server during installation

ECAD translators

- ECADtranslator 17.x
 - It is a common installation Add-on package that will install ANSYS menu in your layout tool. After ECADtranslator installation, a user should see an ANSYS menu item in Cadence Allegro SIP /APD and can translate a layout file to SIwave with Alinks or create an .anf file.

• Slwave installation

- Install **Electronics** primary package : All EM tools will be installed at the same time.

ANSYS Importing a Layout with ALinks from Mentor

🔕 🛃 ڬ 🚔 🚽 🥙 🤍 🕫		Untitled - SIwave
FILE IMPORT HOME EDIT GEOMETRY CIRCUIT ELEMENTS VIEW	ISIBILITY TOOLS EXPORT SIMULATION RESULTS	
Cadence Allegro/APD/SiP Mentor Board Station RE/XE Design ODB++ Design DXF Mentor Expedition Design Zuken CR5000 Design CDB++ (EF7.9.1 or later)	ANSYS EDB C XFL File Apache CPM/PLG AnsoftLinks6 Project Template File APD/SiP Bondwi ANF MDI File	C File B Huray Roughness Models RLC Part Values e Profile File A Layer Stackup S Settings File
HKP (up to EE2007.8)	ANSYS EDA Layouts	Other Imports
	t ODB++ Design ++ archive type: Directory ++ design: C:/Windows/system32/ Brows Be control file: C:/Windows/system32/ Edit / Create XML Control File Import Can	

- Path to import Mentor ODB++ layouts:
 - Import > Mentor Expedition Design > ODB++ (EE7.9.1 or later)

ANSYS Importing a Layout from a ODB++ Design



- Path to import ODB++ layouts:
 - Import > ODB++ design

ANSYS Importing a Layout with ALinks from Zuken

🔕 🛃 ڭ 🗋 🗳 🖉	(° =						Untitled - S	Iwave	
FILE IMPORT HO	ME EDIT GEOMETRY CIRCUIT	ELEMENTS VIEW VISI	BILITY	TOOLS EXPORT	SIMULATION RESU	ULTS			
Cadence Allegro/APD/SiP	🌌 Mentor Board Station RE/XE Design.	🤤 ODB++ Design		ANSYS EDB	📑 XFL File	🛐 Apache CPM/F	LOC File	🛐 Huray Roughness Models	S RLC Part Values
DXF	🏧 Mentor Expedition Design 🔻	🞽 Zuken CR5000 Design		AnsoftLinks6 Project	📑 Template File	🖄 APD/SiP Bond	wire Profile File	. 🔺 Layer Stackup	🖄 Settings File
GDSII	🏧 Mentor Pads Design	Leadframe Editor	ANF	MDL File		🖹 Component Fi	le	🐴 Plane Extents	ind Temperature Profile: Import New Profile 🔻
	Third Party EDA Layouts			ANSYS EDA Layou	JIS .			Other Import	5
			Ope	n Organize Vew folder Favorites Desktop Desktop Downloads Recent Ploces Libraries Documents Music Pictures Videos Computer File nam	C:) ALinks_Training Name 2_ALinks_Exported_2.1 2_ALinks_Exported_2.2 ALinks_Example_hfsan ALinks_Example_sivasu References isignoise_run Solved examples		icarch ALinks_Train imodified (2012 6:31 PM (2012 6:31 PM (2012 3:21 PM (2012 3:21 PM (2012 3:22 PM (2012 3:22 PM (2012 3:04 PM (201	ing Type File folder File folder Fil	

- The recommended path to import Zuken layouts:
 - Import > ANF...
- Otherwise use the ASCII files exported from Zuken (.pcf & . Ftf)
 - Import > Zuken CR5000 design...
- 15 © 2015 ANSYS, Inc. December 7, 2016



How to translate Cadence database to ANSYS tools?

- Two Modes of Operation :
 - Direct Launch from 3rd party layout tool
 - Requires installation of ECAD Integrations executables (ECADtranslator)
 - Stand Alone Editor
 - Export / Import of .ANF files

Here is the view of this integration inside of Cadence APD



ANSYS Cadence Layout Translation

Before Integration

😹 AI	legro F	PCB Per	formar	ice opt	tion	L: ML60	05_BRD.b	ord Proje	ect: F:/	11/SIwa	ve_Update	PCB					
<u>F</u> ile	Edit	View	Add	Displ	ay	Set <u>u</u> p	<u>S</u> hape	Logic	Place	Route	Analyze	Mai	nufact	ure	Tools	Help	р
			÷	C	×	\$	± €	些 🔎	*			Q	•	Q	S	3	0
				-									+	++	1.0,0*1	4	1

After the Integration

😹 AI	legro l	PCB Pe	rformar	nce op	tion	L: unna	med.	brd F	Project	F:/11	/SIwave	e_Upd	late/Po	СВ							
<u>F</u> ile	Edit	View	Add	Displ	lay	Set <u>u</u> p	Sha	ape	Logic	Place	Rout	e Ar	naly <u>z</u> e	Mar	nufact	ure	Tools	ANS	SYS	Help	
			÷	C	×	9	*	¢ 1	9	*	×	图	Q	Q	•	Q	S	3	\odot	30	
				-		0							*			++	* <u>0,0</u> *	1	1	. 0	X

1) Direct link to Slwave with Alinks

Cadence and ANYS EM tools are available on the same machine

ANSYS Help	
A <u>L</u> inks	Launch SIwave with ALinks
HFSS •	Launch TPA
ANSYS Website	Write Ansoft Neutral File V2
	write Siwave Component File



- 2) Write an .anf file and then import it into Slwave with Alinks
- Cadence and ANYS EM tools are installed on different machine

ANSYS Help							
A <u>L</u> inks	Lau	unch SIwave with ALinks					
HFSS •	Lau	unch TPA					
ANSYS Website	Wr	ite Ansoft Neutral File V2					
	Wr	ite SIwave Component File					

ANSYS When to use *.anf file?

- Direct link from Cadence is not appropriate if Slwave is not installed on the same machine. *.anf (Ansoft Neutral File) is required :
 - Select « Write Ansoft Neutral File v2 »



- To get all components, a .cmp file is also required :
 - Select « Write SIwave Component File »
- Launch Slwave :
 - File > Import > ANF or Component File...



ANSYS Drag & Drop the Cadence project In Slwave

• Select Nets to import.

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FILE IMPORT HOME EDIT GEOMETRY CIRCUIT ELEMENTS VIEW	IBUITY TOOLS EXPORT SIMULATION RESULTS	STYLE 👻 🕖
Cadence Allegro/APD/SiP Mentor Board Station RE/XE Design To DDB++ Design	a ArSYS EUB… a XF He… A Apart Chim. A Apart Chim. A Apart Chim. A Hurg's Coupments Models Net Chart Values	
GDSII GDSII GDSII	ANF MDL File Plane Extents imp Temperature Profile:Import New Profile-	
Third Party EDA Layouts	ANSYS EDA Layouts Other Imports	
Single Ended Nets • + × Components • + ×		Layers 👻 🕂 🛪
Regular Exp: Image: Second	Select nets to import from sizewe_board Indef Net Configuration File Indef Net Configuration File Indef Net Configuration File Int Name Int Data, P.2 Int, Data, P.4 Int, Data, P.4	Image: Solution of the second seco
Messages		₩ ₽ ×
Creating Simave Session log C:\USerS\Tecastro\AppData\Local\Temp\Untitled. OS: Windows 7 Professional Service Pack 1 (Build 7601)	9 A Display output from:	
Loaded material library "C:/Program Files/AnsySEM/AnsySEMJ2.0/Win64/syslib Loaded components from "C:/Program Files/AnsySeMI2.0/Win64/syslib Loaded buffer models from "C:/Program Files/AnsySEMI2.0/Win64/supli Translating Cadence design into AMSYS EDB; please waitfailed! Extracta translator log file saved to C:/Users/fecastro/AppData/Local/Temp Importing Ansoft Neutral File E:\vSVLTraining(trunk)SumAve(hout_files/WSD Type : ASCII unencrypted file generated by unknown layout system	aterials.amat" " iwave_board_translation.log l\siwave_board.anf	
Appending to SIwave session log C:\Users\fecastro\AppData\Local\Temp\Untit Importing Ansoft Neutral File E:\SVN_Training\trunk\SIwave\input_files\WSO	d.log A\siwave_board.anf	
Ready	x -26 yr 28 dx	dy: Units: mm 🗸



ANSYS Slwave GUI





Overview of Siwave GUI



Structural Mechanics

Electromagnetics

Systems and Multiphysics



Slwave GUI

GUI Ease of Use Improvements

- Undo/Redo
- Recent project history
- Net Selection Ease of Use
 - Show only highlighted nets
 - Automated differential net identification
 - Automated extended net (ENET) identification
 - Automated pwr/gnd identification
- Net Properties
 - Net properties by hovering cursor
 - Net filtering
 - Detect close edges
 - Measure
 - Check Net Length
 - Calculate Electrical Properties (R, L, C, G, delay, Zo, ...)
 - Change Trace Width
- Color Mode
 - Color by layer
 - Color by net
 - Control highlighting color
 - Control background color
 - Control lighting
- Interactive Options
 - Z Stretch
 - LMB Pan, Roller Zoom
 - Dynamic Zoom or Fast Zoom
 - View Cross-section
 - Hot Keys (standard ALT/SHIFT/LMB commands)





Show (Hide All Other Nets)

appending is space section in a conserving structure comparison of the proving the space section of the conservation of the space section of the space section of the space space of the space s

Change Net color...

Delete Net Color

Show All Nets

Show

Hide

CLK_312K CMD EXECU

CMD_EXEC

CMD EXEC

CMD EXEC

CSCP_N CSCP_N CSCR_N

- Starting Slwave on Windows
 - Click the Microsoft Start button
 - Select All Programs
 - Select Ansys Electromatgnetics Suite 17.0
 - ANSYS Slwave
- Or Double click on the icon on the Windows Desktop
- Starting Slwave on Linux, Go to the install directory : /opt/AnsysEM/AnsysEM17.0/Linux64/ Siwave



ANSYS Slwave User Interface





Slwave Visibility > Workspaces

- The SIwave window has several optional workspaces:
 - Selection Filters
 - Components
 - Information/Errors/Warnings
 - Messages
 - Layers
 - Nets (Single Ended, Differential, Extended, PWR/GND...)
 - Properties
 - Results

Each window can be Floating or Docking







Changing the View

Toolbar



- Shortcuts
 - Since changing the view is a frequently used operation, some useful shortcut keys exist. Press the appropriate keys and drag the mouse with the left button pressed:
 - ALT + Drag Rotate
 - In addition, there are 9 pre-defined view angles that can be selected by holding the ALT key and double clicking on the locations shown on the next page.
 - Shift + Drag Pan
 - ALT + Shift + Drag Dynamic Zoom



Layers Window

- Layer Selection
 - Select the active layer by clicking on the circular radio button. The active layer is important when geometry is being created in the SIwave interface
- **Fill/Unfill Layers** Show/Hide Layers Planes Traces Pads Vias Toggle between Opaque and Layers Wireframe layer views ŤĚ Circuit Elements Active Layer SURFACE V Show/Hide Layers C L2 V C L3 **V** Click the X to either view or hide a layer L4 \checkmark L5 V L6 To select planes, traces, pads, vias or L7 ☑ circuit elements in a particular layer, select the BASE corresponding check boxes Fill/Unfill Layers
- Click on the icons to hide or view all layers

Selection Filter Window

• Check or uncheck boxes to select certain elements. For example, all types of elements can be selected except for Nets since the box is unchecked

Components Window

- For manufacturer supplied components the name, series number, global parts, circuit elements, and pins can be viewed
- For local components (created and placed by the user) the part name, circuit elements and pins can be viewed







Nets Window

- Select and Deselect Nets by clicking the checkbox. Also, Nets can be selected and unselected by using a Regular Expression. Note that the expression field is case sensitive and that both * and ? are supported. In the following window BLT_* selects all of the BLT_DATA nets
- NOTE: The option Wild Cards must be selected in Tools > Options



Properties Window

- Information displayed in the Properties Window will vary based on the type of object selected
- **Types of Objects that can be selected graphically in the Modeler Window:**
 - **Circuit Elements**
 - Capacitors, Inductors, Resistors
 - Ports, Voltage Probes, Current Sources, Voltage Sources
 - **Board Elements**
 - ICs
 - IOs
 - Discrete Devices
 - Geometry
 - Bond Wires, Pads, Planes, Traces, Vias
 - Nets

	operaco	▼ ÷ ∧
4	Net	
	Name	CLK_125K
	Net Length	Compute
	Visibility	Show
	Color Mode	Layer Color
	Net Color	Edit

Net Properties	
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Properties • * ×					
	Resistor				
	Part Number	RES_4K7_10%			
	Name	R16			
	Value	50 Ohms			
	Visible	True			
	Active	True			
	Compute Sensiti	False			
al.	Terminal Nets				
	Positive	SC_CLK_CNT10			
	Negative	SC_CLK_CNT8			
I Terminals					
	Swap Terminals	Swap			
al.	Layers				
	Positive	SURFACE			
	Negative	SURFACE			

Pı	roperties	▼ ₽ >
4 1 1 1 1	Via	4
	Padstack Name	42C16P
	Top Layer	SURFACE
	Bottom Layer	BASE
	Mirrored Layer	False
	Angle (Degrees)	0
	Operate on Angle	Select Action
	Electrical Properti	Display
	Other Properties	Edit
4	Location	3750.000000, 675
	Х	3750.000000
	γ	675.000000
14	Net Information	
	Name	TCI_TCI1_PR_SWI
	Net Length	Compute

Geometry Properties

Pı	roperties	▼ ₽ ×			
4	IC				
	Part Number	74AC04_SOIC			
	Ref. Des	U51			
	Layer	SURFACE			
	S-parameter mo	None			
	SPICE RLC model	None			
	Die Stack	Edit			
	Pin Groups	Edit			
4	Default Buffer Models				
	Class	None			
	Туре				

Board Element Properties



- Geometry
 - Bond Wires, Pads, Planes, Traces, Vias
- Nets

31

Net Properties

Properties	▲ 廿 ×			
∃ Net				
Name	2N559	¥		
Net Length	Compute	Net Lengths		
Visibility	Show	NetName: 40N4742		
Color Mode	Layer Color	Net Name: 40N4742		
Net Color	Edit	Show this net only		
Geor	netry	List of Lengths		
Properties		Lengths between two net nodes		
- Pad	• • *	1) Pins or		
Padstack Name	60X12	End nodes where no object is		
Laver	TOP	connected		
Mirrored Laver	False	Path 1: 233.9961 Path 2: 169.8961		
Angle (Degrees)	0			
Other Properties	Edit	Paul 5: 04.1000		
	6869.173000 2563.898000			
×	6869.173000	(Select a path, then it'll be highlighte		
Y	2563.898000			
Pin Information				
Device Type	DIE			
Part Name	UCD9240PFC QFP50P14X14	Compute Distance		
Ref. Designator Name	U25	Select two net nodes (arrows) in the graphic window.		
Pin Number	7 TEMP			
Net Information		Net Node 1:		
Name	40N4742	Net Node 2:		
Net Length	Compute	Distance:		
Visibility	Show			
Color Mode	Layer Color			
Net Color	Edit	Close		

Information/Errors/Warning and Messages Window

- Messages
 - General information related to various tasks will be displayed in the message window.
- Information/Errors/Warnings Window
 - Errors must be corrected before running the simulation
 - Warnings should be further investigated but SIwave will run the simulation
 - Information messages should be reviewed

Messages		▼ ₽ ×	
Appending to SIwave session log C:\Users\fecastro\AppDat Importing Ansoft Neutral File E:\SVN_Training\trunk\SIwa Type : ASCII unencrypted file generated by unknown lay	a\Local\Temp\Untitled.log ve\input_files\WS01_1\siwave_board.anf put system		
Importing Ansoft Component File E:\SVN_Training\trunk\SIN 64 capacitors read 1 inductors read 16 resistors read	wave\input_files\W501_1\siwave_board.cmp		
Creating SIwave session log E:\Simulations\siwave\ws01\siwave_board.log OS: Windows 7 Professional Service Pack 1 (Build 7601)		E	
Saved E:\Simulations\siwave\ws01\siwave_board.siw	Information / Errors / Warnings	1 - 30	→ ♯ X
		n layer SURFACE is not attached to any net included in this simulation n layer SURFACE is not attached to any net included in this simulation n layer SURFACE is not attached to any net included in this simulation	on E on on
	 C5: negative node at (825.000000,5125.000000) or C6: negative node at (1225.000000,4575.000000) or 	n layer SURFACE is not attached to any net included in this simulatic on layer SURFACE is not attached to any net included in this simulat	on





Several selecting mode

- Home > Selection
- Right Mouse Button



Units :

- In the Toolbars, set the reference units
 - Usefull for drawing, measurement...

Coordinate of the mouse

• In the Toolbars



ANSYS GUI Controls – Cursor Tool-tip

Cursor tool-tip shows information about the selected object: component, trace, net, device, etc







ANSYS GUI Controls – Via Properties

- Via Properties
 - Graphically select a via in the layout then select the menu item
 - Edit > Via... to bring up the Via Properties Window
 - Editing the properties in this window will override the padstack definition. For example, if a user would like
 to investigate whether or not to backdrill a via on a high-speed net the bottom layer can be changed. The
 antipad definition for a particular via can also be investigated without having to change the parameters of all
 of the other vias that share the same padstack
 - Pin Info provides the Type, Layer, Part Name, Reference Designator and Pin Name for the selected pad. The Part Name, Reference Designator and Pin Names can be edited from here as well

Via Properties		X		
Top Layer	SURFACE	•		
Bottom Layer	BASE	•		
Rotation Angle	0	degrees		
Mirrored?	No 🔻			
Check layer(s) which the selected vias have antipads on As is (Uncheck to select	SURFACE GND SIG1 SIG2	T T		
Pin Info			0	
Type Not	Defined			
Part Name		•		
Ref. Designator		-		
Pin Name				
Delete				
ОК		Cancel		

lia Properties					
Top Layer	SURFACE	•			
Bottom Layer	SURFACE	•			
Rotation Angle	0	degrees			
Mirrored?	No 🔻		S		
Check layer(s) w the selected vias antipads on As is (Uncheck to sele layers)	hich have GND SIG1 SIG2 ct VPP	4 III •			
Pin Info				C	
Туре	DIE				
Layer	SURFACE	•			
Part Name	SQFP28×28_208	-			
Ref. Designator	U1	-			
Pin Name	146				
Delete					
ОК		Cancel			

ANSYS Slwave GUI Controls – Results

Plot Self terms or Transmission terms

• Click on "Select self terms" to quickly plot all the self term



Ideal to plot all the "Reflexions" of the S parameters matrix.

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ANSYS GUI Controls –Script Commands

Any script language that supports ActiveX objects may be used:

- VBScript
- Jscript
- Python

Extensive scripting support allows automation.

Online Help

• Script Commands are available

Realize Your Product Promise™



GUI Controls Visualization



Structural Mechanics

Electromagnetics

Systems and Multiphysics

Performing Faster Transformations

- Slwave allows you to view a simplified model during rotate, zoom or pan operations.
- View>Faster Rotate.
- Planes are represented in 2D, while vias and circuit elements are not displayed while you are rotating, zooming or panning in. The complete design is displayed only after you finish the operation.



Before and After Rotation



During Rotation







Layer Color Mode

A user can toggle between the net and layer color modes



Net Color Mode



two color modes

- Object properties window
 Same antione available using a right of
- Same options available using a right-click on the net list.

- Changing opaque view by setting Translucency for all metal
 - Select all > METAL layers > Apply
 - Set Translucency to 70% > update
 - Better 3D visualization and rotation

LOIO	Name	Туре	⋕ Thickness (mils)	🏠 Material	Conductivity (S/m)	🏠 Dielectric Fill	Dielectric constant	Loss tangent	Translucency	Elevation (mils)	Roughness (mils)
	UNNAMED_1	DIELECTRIC	0	air	0		1.0006	0		52.08	
	SURFACE	METAL	0.72	copper	5.8E+07	air	1.0006	0	70	51.36	HJ: 0 , HJ: 0
	UNNAMED_3	DIELECTRIC	6	FR4_epoxy	0		4.4	0.02		45.36	
	L2	METAL	1.44	copper	5.8E+07	FR4_epoxy	4.4	0.02	70	43.92	HJ: 0 , HJ: 0
	UNNAMED_5	DIELECTRIC	6	FR4_epoxy	0		4.4	0.02		37.92	
	L3	METAL	1.44	copper	5.8E+07	FR4_epoxy	4.4	0.02	70	36.48	HJ: 0 , HJ: 0
	UNNAMED_7	DIELECTRIC	6	FR4_epoxy	0		4.4	0.02		30.48	
	L4	METAL	1.44	copper	5.8E+07	FR4_epoxy	4.4	0.02	70	29.04	HJ: 0 , HJ: 0
	UNNAMED_9	DIELECTRIC	6	FR4_epoxy	0		4.4	0.02		23.04	
	L5	METAL	1.44	copper	5.8E+07	FR4_epoxy	4.4	0.02	70	21.6	HJ: 0 , HJ: 0
	UNNAMED_11	DIELECTRIC	6	FR4_epoxy	0		4.4	0.02		15.6	
	L6	METAL	1.44	copper	5.8E+07	FR4_epoxy	4.4	0.02	70	14.16	HJ: 0 , HJ: 0
	UNNAMED_13	DIELECTRIC	6	FR4_epoxy	0		4.4	0.02		8.16	
	L7	METAL	1.44	copper	5.8E+07	FR4_epoxy	4.4	0.02	70	6.72	HJ: 0 , HJ: 0
	UNNAMED_15	DIELECTRIC	6	FR4_epoxy	0		4.4	0.02		0.72	
1	BASE	METAL	0.72	copper	5.8E+07	air	1.0006	0	70	0	HJ: 0 , HJ: 0
dd / D	L7 UNNAMED_15 BASE elete / Move Layer(s)	METAL DIELECTRIC METAL Edit Selec	1.44 6 0.72 tted Layer(s)	copper FR4_epoxy copper	5.8E+07 0 5.8E+07	FR4_epoxy air	4.4 4.4 1.0006	0.02 0.02 0	70 70	6.72 0.72 0	
Add	Above Selected Layer	Color	As Is	Update	Dielectric Fill As	Is	▼ Update				
Ad	d Below Selected Layer	Name	As Is	Update	Translucency	()	70% Update				
Mo	ve Selected Layers Up	Туре	METAL	▼ Update	Thickness As	Is	mils Update				
Mov	e Selected Layers Dowr	n Material	copper	▼ Update	Roughness	HJ: 0 , HJ: 0	mils Update				



View > Compute Cross Section

• Draw a clipping line



• View > Back To Full Design







• View > View Options

- Z Stretch– artificially scale Z values so that very thin planar objects have a 3D appearance. Choose any discrete value between 1 to 25
- Change Selection Color change default selection color (yellow)
- Circuit Element Size change the scale factor for circuit elements
- Gradient Background change default background colors
- Lighting change the Brightness and Contrast

	Color	Gradient Background Editor
	Basic colors:	Gradient background settings Customize Default
✓ Adaptive Grid Spacing ✓ </td <td></td> <td>Top Color</td>		Top Color
View Options Set the scale factor of circuit elements	Hue: 40 Red: 255 Sat: 240 Green: 255 Color/Solid Lum: 120 Blue: 0 OK Cancel Add to Custom Colors	Preview
1 x Lighting I	Properties 20 Intrast 50	Bottom Color
OK Apply Cancel	Default OK Cancel	OK Cancel

• Stretching Z :

- To artificially scale Z values, so that very thin planar objects have a 3D appearance.
- View>View Options>Z Stretch.
- Choose any discrete value between 1 to 25, as the scaling factor.



Original view : scaling factor = 1

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Original view : scaling factor = 10

ANSYS GUI Controls – Simplify Visualization

• View > Simplify Circuit Elements





Simplify Circuit Elements



• View > Simplify Vias









ANSYS GUI Controls – Simplify Visualization



• Unfill All layers by clicking on the yellow rectangle in Layer workspace





- To improve the response time when Slwave is running over a remote desktop:
 - OpenGL management is mandatory to support 3D
 - Informational tooltips will not appear.
 - Dynamic zoom is deactivated.
 - Faster transformation is activated.
 - Simplify all visualizations settings :
 - Vias
 - Circuit Elements
 - 2D view for layers
 - Use Translucency / Unfill layers





Syntax for Slwave:

<path to>/siwave -exec_eigen <path to>/<project name>.siw

The following flags are supported:

-exec_eigen

-exec_syz

-exec_ac

-exec_dc

Examples :

C:\instaldir\siwave -exec_syz D:\Examples\Midplane.siw

C:\instaldir\siwave -exec_eigen D:\Examples\switch.siw

C:\instaldir\siwave -exec_dc D:\Examples\Blade.siw

ExecAcSim ExecResModeSim ExecPdnSim ExecPsiPdnSim ExecSyzSim ExecSentinelPsiSyzSim ExecSentinelPsiAcSim ExecFfSim ExecFfSim ExecCfSim ExecCSim ExecFwsSim ExecFwsSim

ANSYS Non graphical Batch solve command

In R16, siwave_ng can be used as follows :

• This command, in addition to executing a requested simulation type, creates the necessary directory hierarchy and .asol file such that results can be post-processed in the UI after the siwave_ng run completes.

siwave_ng <path to .siw> <path to .exec> -formatOutput -useSubdir

Example :

C:\Program Files\AnsysEM\AnsysEM16.2\Win64\siwave_ng C:\projects\ssn.siw C:\test\execsyz.txt -useSubdir

ExecSyzSim

SetSwp 5e3 5e9 500 Linear

The .exec file, at the very least, should contain one of the following strings (which specify the type of analysis to execute):

ExecAcSim ExecResModeSim ExecPdnSim ExecPsiPdnSim ExecSyzSim ExecSentinelPsiSyzSim ExecSentinelPsiAcSim ExecFfSim ExecNfSim ExecDcSim ExecFwsSim ExecPiOptSim This file can also (optionally) contain commands to modify the sweep, change the number of CPUs, the licensing scheme, etc.:

SetSwp SetNumCpus AddSwp SetInterpSwp SetDiscreteSwp InterpSwpCvg NumInterpPts EnableQ3dDomains WaitForLicense DistributeSIwaveSyz HpcHostName ComputeExactDcPt SolverMemLimit UseHpcLicenses

ANSYS Non graphical Batch solve in detail

SetSwp <f start> <f end> <num pts> <linear/log/linear step InterpSwpCvg 0.005 SetSwp 0 1e9 100 Linear NumInterpPts <num points> - number of points to be explicitly solved for during the interpolating sweep AddSwp <f start> <f end> <num pts> <linear/log/linear step> NumInterpPts 30 - use this like you are adding another sweep line in the UI; allows for changes to the number of points & the distribution type • UseHpcLicenses <pack | pool> - use in conjunction with SetSwp - SolverMemLimit <% of memory to be used by the solver on a machine when using a HPC SetSwp 0 1000 10 Log License> AddSwp 1000 5e9 500 Linear **UseHpcLicenses pack** SolverMemoryLimit 80 SetNumCpus <number> ComputeExactDcPt <boolean> SetNumCpus 4 ComputeExactDcPt 1 . SetDiscreteSwp EnableQ3dDomains <boolean> - no argument; just tells the simulation to use a discrete sweep for the sweep setup in EnableQ3dDomains 1 the UI - can also use in conjunction with SetSwp WaitForLicense <boolean> SetSwp 0 1e9 100 Linear WaitForLicense 1 **SetDiscreteSwp** DistributeSIwaveSyz ٠ SetInterpSwp no argument required - no argument; just tells the simulation to use an interpolating sweep for the sweep setup in the UI HpcHostName <machine_name | IP address> <CPUs_to_use> <%Memory> - can also use in conjunction with SetSwp - use in conjunction with DistributeSIwaveSyz SetSwp 0 1e9 100 Linear - can use this command to enter multiple machines DistributeSIwaveSyz SetInterpSwp HpcHostName \\machineA 6 80 HpcHostName \\machineB 6 80 HpcHostName \\machineC 6 80

InterpSwpCvg <Relative error for S>



Stack up, Padstack, Balls/Bumps, Bondwire

Fluid Dynamics

Structural Mechanics

Electromagnetics

Systems and Multiphysics

ANSYS Layer Stack-up Editor

• All layers are imported with material properties and thickness

lor	Name	Туре	Thickness (mils)	🏝 Material	Conductivity (S/m)	🏝 Dielectric Fill	Dielectric constant	Loss tangent	Translucency	Elevation (mils)	Roughness (mils)
	UNNAMED_1	DIELECTRIC	0	air	0		1.0006	0		52.08	
	SURFACE	METAL	0.72	copper	5.8E+07	air	1.0006	0	70	51.36	HJ: 0 , HJ: 0
	UNNAMED_3	DIELECTRIC	6	FR4_epoxy	0		4.4	0.02		45.36	
	L2	METAL	1.44	copper	5.8E+07	FR4_epoxy	4.4	0.02	70	43.92	HJ: 0 , HJ: 0
	UNNAMED_5	DIELECTRIC	6	FR4_epoxy	0		4.4	0.02		37.92	
	L3	METAL	1.44	copper	5.8E+07	FR4_epoxy	4.4	0.02	70	36.48	HJ: 0 , HJ: 0
	UNNAMED_7	DIELECTRIC	6	FR4_epoxy	0		4.4	0.02		30.48	
	L4	METAL	1.44	copper	5.8E+07	FR4_epoxy	4.4	0.02	70	29.04	HJ: 0 , HJ: 0
	UNNAMED_9	DIELECTRIC	6	FR4_epoxy	0		4.4	0.02		23.04	
	L5	METAL	1.44	copper	5.8E+07	FR4_epoxy	4.4	0.02	70	21.6	HJ: 0 , HJ: 0
	UNNAMED_11	DIELECTRIC	6	FR4_epoxy	0		4.4	0.02		15.6	
	L6	METAL	1.44	copper	5.8E+07	FR4_epoxy	4.4	0.02	70	14.16	HJ: 0 , HJ: 0
	UNNAMED_13	DIELECTRIC	6	FR4_epoxy	0		4.4	0.02		8.16	
	L7	METAL	1.44	copper	5.8E+07	FR4_epoxy	4.4	0.02	70	6.72	HJ: 0 , HJ: 0
	UNNAMED_15	DIELECTRIC	6	FR4_epoxy	0		4.4	0.02		0.72	
	BASE	METAL	0.72	copper	5.8E+07	air	1.0006	0	70	0	HJ: 0 , HJ: 0
De	lete / Move Layer(s)	Edit Select	ted Layer(s)		_						
uu	Above Selected Layer	Color	As Is	Update	Dielectric Fill As	Is				# 8	
\dd De	l Below Selected Layer elete Selected Layers	Name	As Is	Update	Translucency		70% Update				
1 0١	/e Selected Layers Up	Туре	METAL	▼ Update	Thickness As	Is	mils Update				
ove	e Selected Layers Dow	n Material	copper	▼ Update	Roughness	HJ: 0 , HJ: 0	mils Update				

- Possible to edit and export/import the Layer stackup (".stk" file)
 - File > export > Export Layer Stackup



• Easily change the material properties using the predefined Material library of Slwave or Add a new one.

🔳 La	yer St	ackup Editor				0	1		111		IN I	Cherry		
	Color	Name	Туре	✤ Thickness (mils)	🔈 Material	Conductivity (S/m)	Dielectric	Fill	Dielectric const	tant Loss tangent	Translucency	Elevation (mils)	Roughness (mils)	
		UNNAMED_1	DIELECTRIC	0	air	0			1.0006	0		52.08		
►		SURFACE	METAL	0.72	copper	5.8E+07	air		1.0006	0	0	51.36	HJ: 0 , HJ: 0	
		UNNAMED_3	DIELECTRIC	6	copper 🗸	. 0			4.4	0.02		45.36		
		L2	METAL	1.44	gold	5.8E+07	FR4_epoxy		4.4	0.02	0	43.92	HJ: 0 , HJ: 0	
		UNNAMED_5	DIELECTRIC	6		0			4.4	0.02		37.92		
		L3	METAL	1.44	indium	5.8E+07	FR4_epoxy		4.4	0.02	0	36.48	HJ: 0 , HJ: 0	
		UNNAMED_7	DIELECTRIC	6	INVAR	0		Material Prop	erties					
		L4	METAL	1.44	Iron KOVAR	5.8E+07	FR4_epoxy							_
		UNNAMED_9	DIELECTRIC	6	lead	0		Conductors	Dielectrics					
		L5	METAL	1.44	magnesium	5.8E+07	FR4_epoxy							
		UNNAMED_11	DIELECTRIC	6	MONEL	0		Name		Relative Permittivit	ty Lo	oss Tangent	Measurement Frequency	y (Hz)
		L6	METAL	1.44	mu_metal	5.8E+07	FR4_epoxy	AG_C	U_EUTECTIC	4.5	0		1E+09	
		UNNAMED_13	DIELECTRIC	6	NdFe30	0		📔 🔒 air		1.0006	0		1E+09	
		L7	METAL	1.44	NdFe35	5.8E+07	FR4_epoxy	📔 🔒 Al2_C	3_ceramic	9.8	0		1E+09	
		UNNAMED_15	DIELECTRIC	6	nickel	0		A_N		8.8	0		1E+09	
		BASE	METAL	0.72	palladium	5.8E+07	air	ALUN	IINA	10	0		1E+09	
					pec			alumir	na_92pct	9.2	0.	800	1E+09	
Ac	dd / De	elete / Move Layer(s)	Edit Selecte	d Layer(s)	PLATED COPPER FOIL				ла_эррст	9.4	U. 0	006	1E+09	
	Add	Above Selected Layer	Color		platinum	Dielectric Fill		ALON Adop	25ER (m)	0.0 3.59	0	0035	1E+03	
	Ado	Below Selected Layer			rhodium			Arlon	25N (tm)	3.38	0.	0025	1E+09	
	D	lata Calacted Lavara	Name		silver — SmCo24	Translucency		Arlon	AD1000 (tm)	10.2	0.	0023	1E+09	
	Di	Bete Selected Layers			SmCo28	Thickness		🛛 🔒 Arlon	AD250A (tm)	2.5	0.	0015	1E+09	
	Mo	ve Selected Layers Up	Type		solder	Thickness								
	Move	e Selected Layers Dowr	n Material		STAINI ESS STEFI	Roughness		Add	Dele	ete Modi	fy			
Selec	ct all	DIELECTRIC - lay	ers Apply	Edit Material Proper	ties Invert Stackup	Conformal Coat	Units mil					0	K Cancel	Hel

• Add a new Material

• You can click on Edit Material Properties > Add... or go to Home > Edit Materials



ANSYS Materials – View / Edit /Create

Materials

- View existing material properties or create a new material
- Make sure that the correct material, Conductor or Dielectric, is selected then click the Add button to create a new material

lame	Relative Permittivity	Loss Tangent	Measurement Frequency (Hz)
AG_CU_EUTECTIC	4.5	0	1E+09
AIR	1	0	1E+09
air	1.0006	0	1E+09
AI2_O3_ceramic	9.8	0	1E+09
AI_N	8.8	0	1E+09
ALUMINA	10	0	1E+09
alumina_92pct	9.2	0.008	1E+09
alumina_96pct	9.4	0.006	1E+09
ALUMINUM_NIT	8.5	0	1E+09
Arlon 25FR (tm)	3.58	0.0035	1E+09
Arlon 25N (tm)	3.38	0.0025	1E+09

Dielectrics

- Choose which dielectric material model to use
- The preferred Djordjevic-Sarkar model is a causal frequency-dependent dielectric model developed specifically to model FR-4. It is also useful for many other low-loss insulator materials. The Debye model characterizes a lossy dielectric material by two measured values at a certain frequency. (More detailed information on both of these models can be found in the Slwave Help)

	Edit D-S Material Properties		
	Name: NewDielectric		Material Name NewDielectric Low Frequency Parameters
		E	Frequency (Hz) 1E+06
Select dielectric material model to use	Relative Permittivity:		Relative Permittivity 2
	Conductivity:	0 S/m	DC Conductivity (Siemens)
 Djordjevic-Sarkar (preferred) 	Properties at Measurement Fr	requency	- High Frequency Parameters
C Debue	Measurement Frequency:	1E+09 Hz	
0.000,0			Frequency (Hz) 1E+09
	Relative Permittivity:	4	Relative Permittivity 1
OK Cancel	Loss Tangent:	0.02	Optical Relative Permittivity
			Loss Tangent 0.002
55 © 2015 ANSYS, Inc. December 7, 2016	ОК	Cancel	OK Cancel

ANSYS Material - Frequency dependent parameter

- Have to consider :
- Conductor loss
 - Skin Effect
- Dielectric constant and loss
 - Djordjević-Sarkar model

$$\varepsilon(\omega) = \varepsilon'(\omega) + j\varepsilon''(\omega)$$
$$= \varepsilon_{\infty} + \frac{\Delta\varepsilon}{\ln(\omega_{B}/\omega_{A})} \ln\left(\frac{\omega_{B} + j\omega}{\omega_{A} + j\omega}\right) + \frac{\sigma}{j\omega\varepsilon_{0}}$$



Frequency dependent models are default





- Define Trace Cross Section by choosing the appropriate shape by layer:
 - Rectangular, Trapezoidal and hexagonal

- Hexagon Trapezoid Rectangle × Trace Cross Section Shape Editor × x Trace Cross Section Shape Editor Trace Cross Section Shape Editor Laver: SURFACE -Layer: SURFACE Layer: SURFACE • • Shape: Hexagon • Shape: Rectangle • Shape: Trapezoid • W1 W1 Etching Style Etching Style Etching Style Over Etch Over Etch Over Etch O Under Etch O Under Etch O Under Etch Width Formula (Trapezoid Only) Formula (Trapezoid Only) Formula (Trapezoid Only) W2 W1 = Width * N/A W1 = Width * N/A W1 = Width * 0.85 Width W1 = Width - N/A * Thickness W1 = Width - N/A * Thickness W1 = Width - 0.85 * Thickness Set Ratios Set Ratios Set Ratios Set Absolute Values For Etching Set Absolute Values For Etching Set Absolute Values For Etching Top: Top: -0-Top: W1: W1: W1: 100 % 85 % 85 % W2: W2: W2: Bottom: Bottom: Bottom: 100 % 85 % 85 % Slide Both Simultaneously Slide Both Simultaneously Slide Both Simultaneously OK Cancel OK OK Cancel Cancel
- Edit > Trace Cross Section...

ANSYS Trace Electrical Properties

- Display the electrical properties of the selected transmission line in real time.
- Selecting mode should be on "object"
- In the properties window, click on Display



ANSYS Bondwire Electrical Properties



ANSYS Padstack Editor

• Padstacks describe the stacking structure of shapes associated with pads and vias. They enable different shapes on different layers and contain drill information, plane layer information, and inner layer information. In the editor, padstacks can be added, modified or deleted

adstack

Home > Edit Padstacks

• Select a padstack to view its properties. If a via is selected in layout it will automatically be highlighted when the Padstack Editor is launched

	35070N 350106N 350110N 350125N 350180N 38016P 42016P 42016P 42016P	Delete Padstack	Copy Padstack	Via Pl Ra Ab	k Properties 35C70N ating tio solute 7 mits	Via Material brass bronze cast_iron chromium cobalt copper gold
1 1	Layer	Pad	Antip	ad	Thermal Relief Pad	
	SUBFACE	Circle (B: 17.5)	Circle	(B: 75)	Circle (B: 75)	
	UNNAMED 3	Circle (R: 35)	None		None	
	L2 -	Circle (R: 17.5)	Circle	(R: 75)	Circle (R: 75)	
	UNNAMED_5	Circle (R: 35)	None		None	
	L3	Circle (R: 17.5)	Circle	(R: 75)	Circle (R: 75)	
	UNNAMED_7	Circle (R: 35)	None		None	
	L4	Circle (R: 17.5)	Circle	(R: 75)	Circle (R: 75)	
Fan Dawe Mare	UNNAMED_9	Circle (R: 35)	None		None	
op-Down view	L5	Circle (R: 17.5)	Circle	(R: 75)	Circle (R: 75)	
	UNNAMED_11	Circle (R: 35)	None		None	
	L6	Circle (R: 17.5)	Circle	(R: 75)	Circle (R: 75)	
	UNNAMED_13	Circle (R: 35)	None	•	None	
	Select All Meta	Layers Se	lect All Dielectric Layer	s		
	Pad Properties		Antipad Properties		Thermal Relief Pad Properties	
	Shape: Circle	•	Shape: Circle	-	Shape: Circle	•
Polygonal Pad Edit	Radius: 17.5	mils	Radius: 75	mils	Radius: 75	
P A T	Height:	mils	Height:	mils	Height:	

ANSYS SolderBall Generation

• Home > Solderball Properties



• Choose padstack and Enter Type, Radius and Height

Solderball Properties			X
Type: Complex Material: solder	Color:	Padstacks 185_140R 185_140RPIN1 270_95R 35CT06N	
Solderball Placement Solderball Placement Above Layer Stackup Below Layer Stackup	Terminal Type All solderballs are sinks All solderballs are sources Leave types as is	35C110N 35C125N 35C180N 35C70N 36C16P 42C16P 602,45R 68C37P 68537P 68537P 68537P 68537P 68530P 70,35RP1M 75,35PP1M 75,35PP1M 75,35PP1M 75,35PP1M 75,35PP1M 75,35PP1M 75,35PP1M 75,35PP1M 75,35PP1M 75,35PP1M 75,35PP1M 75,35PP1M 75,35PP1M 75,35PP1M 75,35PP1M 75,35PP1M 75,35PP1M 75,35PP1M 75,35PP1M 75,55PP1M 75	
Solderball Dimensions Height: Radius: Frustum Height: Middle Radius:	60.000000 mils 21.600000 mils 20.000000 mils 27.000000 mils	00-55R 90_12R 90_12RPIN1 90_35R 90_35RPIN1 CMP_FIDUCAL TC68C28P TC68C28P	
		OK	Cancel



Creation of the solderballs and add a PCB layer

• Update the stackup (replace FR4 by Air)

Color	Name	Туре	🆄 Material	Translucency	Thickness (mils)	Elevation (mils)	Roughness (mils
	Top Dielectric	DIELECTRIC	air		0	29.26	
	SURFACE	WIREBOND	copper		0	29.26	
bbbt	00 TOP_COND	METAL	copper	65	1.44	27.82	0,0
	UNNAMED_4	DIELECTRIC	FR-4		3	24.82	
6963	69 VCC	METAL	copper	65	1.44	23.38	0,0
	UNNAMED_6	DIELECTRIC	FR-4		5	18.38	
📕 1b8d	aa GND	METAL	copper	65	1.44	16.94	0,0
	UNNAMED_8	DIELECTRIC	FR-4		3	13.94	
📕 ff 804	0 BASE	METAL	copper	65	1.44	12.5	0,0
	Bottom Dielectric	DIELECTRIC	 FR4_epoxy 	-	11.811	0.688976	
377:	Of 🔹 Slwave PCB	METAL	- copper	- 65	0.688976	0	0.0

ANSYS Bondwire Generation

- Bondwire models can be assigned to the layers in the stackup. This command is active only when at least one layer has the type **WIREBOND**. You can edit the layer properties to change the layer type.
- Because bondwires are modeled as traces, you first need to draw a trace before creating a bondwire.
- Edit > Bondwire Model



23 Bondwire Model Editor 🔳 🔛 🔛 0.2 Typical Bondwire Len: 2 mm Model Name: test Type: JEDEC 4-Point x: -0.6 y: 1.4 dx: dy: Flip Profile Across XY-Plane Diameter: 0.1 Reverse Pkg & Die h1: 1 mm Static Diagram Select Bondwires h2: 0.5 degrees alpha: Create New Model degrees Delete Current Model Edit Profile Points... Apply OK Cancel





ANSYS User Defined Bondwire for SiP

- For Bondwire profile, it is common to use JEDEC 4 or 5 points, but this can cause collision problem for stacked dies in SiP.
- With User Defined Bondwires is it possible to draw every kind of profile from sketch (user can also edit, save or import his own profile)



										- 11		х	Z	Segment Le
Lauer 11/IP	CDOND		_	Madel	Skata	hod		-			1	24.400463	197.772171	
Layer. I win	CDUND	_	-	Huder	Javeco	neu		-			2	25.684697	241.436156	43.682867
											3	77.054092	273.542028	60.577238
										П	٠	314.637544	285,100142	237.864429
										П	5	399.397046	268.405089	86.398066
· ·			<u> </u>							П	6	476.451139	213.182989	94.798805
	-									П	7	498.283131	150.255480	66.607111
/											0	500.000000	100.000000	50,284798
											9	500.000000	50.000000	50,00000
									٩k			-Add new ve	rtex	
Radius: 10		icions		alpha:			1985	Ì	tic			Add new ve	rtex	Below
Radius 10	ſ	icions		alpha:		deg	, Jees	Ì,	14			Add new ve	rtex	Below
Radius: 10	fr T	icions		alpha; beter		deg	1 ses	Ì,	*14			Add new ve Above.	rtex	Below
Radius: 10 H1 H2: 147.	r 77217 m	icions icions	Supp	alpha: beta: ort	TOP_CI	deg deg OND	yees Jees),	*			Add new ve Above, Delete verte Selected	rtex	Below Al
Radius: 10 h1 h2: 147. Filo Profile/	п п 77217 п Астова XY	icions icions icions icions	Supp Layer Termi	alpha: beta ort c	TOP_CI	deg deg OND	yees yees		*			Add new ve Above, Dekte verte Selected Upd	rtex	Below Al

idit Bondwire Profile Vertices Al coordnate values are in microns

ANSYS Custom Bondwire Profile

• Edit > Bondwire Model...

Create a custom bondwire profile by entering points or importing coordinates from a file. The .bwp (bondwire profile) can be imported for use in other projects. Click the Update Bondwire Diagram button to refresh the sketch

		Edit Bondwire Profile Vertices	
Bondwire Model Editor - Typical Bondwi	re Len: 0.5 mm	All coordinate values are in mm	
		Segment lengths in red are less than 3 times	📭 Bondwire Model
		meshing problems.	
Model Name: Bridge 🗸	Type: Sketched		
		X 2 Segment Length	
		² 0.123712 0.330000 0.311130	
		3 0.371137 0.330000 0.247425	
	· · ·	4 0.453612 0.030000 0.311130	
- <u>/</u> · · ·	· · · · · ·		
die .	Pkg		
		Add new vertex	
			# File created by Ansoit TPA
Diameter: 0.02 mm	Flip Profile Across XY-Plane	ADOVE	# Sketched bondwire profile point data
bt/	Reverse Pkg & Die	Delata vertav(a)	<pre># Project: GSG_model.tpa</pre>
mm			# Bondwire layer: Bridge
h2: 0 mm	Bridge	Selected All	
			UNITS mm
alpha;degrees	Create New Model	Update Bondwire Diagram	0.041237 0.030000
beta: degrees	5 Delete Current Model		0.123712 0.330000
		Export Profile Import Profile	0 371137 0 330000
Edit Profile Points	OK Cancel		0.452612.0.020000
		OK Cancel	0.133012 0.030000
© 2015 ANSYS, Inc.	December 7, 2016		



ANSYS Relocate Bondwires

- Tools > Relocate Bondwires...
- One isolated Bondwire « VDD_LNA » on Layer 'WB11'
- Relocate it on 'WB22' layer using « Relocate Bondwires » utility

		N N D	Properties	▼ ₽ ×
-			Bondwire	
- Delocate Rondwires			Layer Name	WB11
Nº Relocate Dolluwires			Length (microns)	1055.87
-			Bondwire Model	WB11
			Support Layer	M1
			Termination Layer	WB11
		AAAAA	Orientation	Correct
		KHKR	Center Line	Edit
			Electrical Propert	Display
			Net Information	100 1114
			Name	VDD_LNA
	Relocate Bondwires		Net Length	Compute
			Visibility Color Mode	Snow
	Relocate Selected Bondwires		Net Color	Edit
			Her color	Luit
	Relocate Bondwires By Length			
	Length Criteria (in microns)			
	U < Bondwire Length < 0			
		h La h		
	Destination Laver: WB22			
	WDZZ			
	OK Cancel			
		J		

Realize Your Product Promise™



Drawing Mode

Fluid Dynamics

Structural Mechanics

Electromagnetics

Systems and Multiphysics

ANSYS Drawing Mode (1/2)

To modify the layout, you can specify various options for drawing two or more geometric shapes. The shapes can be either added without merging, or merged, or subtracted.

Select one of the three mode

- Draw > Drawing Mode
 - Add (No Merge) : To draw and display multiple objects together. No union between each shape primitive and different "net name".
 - Merge : To draw and display multiple objects as one merged object. Same "net name".
 - Subtract : An existing geometry can be modified by drilling holes in it or by removing some elements from it. The area of the geometrical shape is cut out from the main Drawing Area.



ANSYS Drawing Mode (2/2)

Select the drawing layer in the Layers Workspace

Select a primitive :

- Circle (Shortcut Key: F5)
- Polygon (Shortcut Key: F6)
- Rectangle (Shortcut Key: F7)
- Trace (Shortcut Key: F8)
- Via (Shortcut Key: F9)

Note 1 : To draw a Trace

- Specify the width before
 - Draw > Set Trace Width...

Note 2 : To draw a Via

Select a Padstack before





ANSYS Measuring Data

- Slwave allows you to measure the distance between points and spacing between edges.
- To measure data :
 - Click Tools>Measure. The Measure Data dockable window appears.
- To measure the distance between two points: Click any point for a reference coordinate. This is displayed as Position 1. Move the cursor in the Drawing Area to see the values for Position 2 and Distance between Points. The data updates as the cursor is moved. The shape of the cursor changes when it is snapped to a corner or mid-point.
- To measure the shortest distance between two edges: Select an edge in the Drawing Area. This is displayed as the Reference Edge. Move the cursor over another edge to see the values for Current Edge and Shortest Distance.

Measure Data			×
4	Position 1 (Reference)		
	Х	0.000000	
	γ	0.000000	
	Layer	METAL-2	
4	Position 2 (Current)		
	Х	-11.998424	
	γ	8.412258	
	Layer	METAL-2	
4	Distance Between Points		
	Distance	14.653609	
	dx	-11.998424	
	dy	8.412258	
	dz	0.000000	
4	Spacing Gap Between Edges		
	Reference Edge	Please select	
	Current Edge	Not available	
	Shortest Distance	Not available	

ANSYS Computing Net Length

- You can compute the lengths of all possible paths in a net, and also calculate the distance between any two net nodes.
- **Tools > Compute Net Lengths or « Compute » button in the properties** window




 Boolean operations can be performed on planes. You can unite, intersect or subtract planes.



Eg : Uniting Planes

- Select the two planes that you want to unite.
- Click Edit>Boolean Operations>Unite.







ANSYS Edit Trace/Bondwire center line properties

• Trace/Bondwire

 To edit a bondwire first graphically select a bondwire in the layout. Bondwire coordinates can be edited. The bondwire radius is also displayed

Edit Trace	Layers 👻 🕂 🛪	Edit Bondwire	
X Y Width Arc Center X Arc Center Y CW 1 10.164850 -0.088230 0.040000 Image: Center X Arc Center Y CW 2 0.066670 0.134100 0.040000 Image: Center X Arc Center Y CW 3 0.083130 0.267210 0.040000 Image: Center X Arc Center Y CW 4 0.216320 0.400400 0.040000 Image: Center X Arc Center Y CW 5 0.674360 0.400400 0.040000 Image: Center X Arc Center Y CW 6 0.719960 0.421040 0.040000 Image: Center X Image: Center X Image: Center X 7 1.228130 0.506700 0.040000 Image: Center X Image: Center X Image: Center X 8 1.298140 0.506840 0.040000 Image: Center X Image: Center X Image: Center X	METAL-5 X V V V METAL-1 X V V V METAL-2 X V V V METAL-3 X V V V METAL-4 X V V V	X Y Width Arc Center X Arc Center Y CW 1 0.300000 -0.685000 0.010000	Image: Constraint of the state of the st
Add new vertex Edit trace width Above Below Delete vertex(s) Image: Constraint of the second seco	Properties 👻 म 🛪	Add new vertex Edit trace width Above Below Delete vertex(s) All Nodes Selected All	Properties
Cross Section Shape Cross Section Shape: Rectangle Height: 0.027 mm Width: 0.04 mm	A Trace Layer METAL-2 Length (mm) 2.330991 Width (mm) 0.100000 Center Line Edit Electrical Properti Display A Net Information Name Name NET_1 Net Length Compute Visibility Show Color Mode Layer Color	Cross Section Shape Cross Section Shape: Circle The radius is 0.01 mm Switch Vertices OK Cancel	Termination Layer METAL-5 Orientation Correct Center Line Edit Electrical Properti Display Met Information Net Information Name NET_2 Net Length Compute Visibility Show Color Mode Layer Color Net Color Edit

ANSYS Edit Plane / Solderball properties

• Plane (Boundary/Cutout)

 Manually edit plane boundaries. To activate this option graphically select a plane

- Solderballs
 - Create solderballs and/or solderbumps on packages. Choose the Padstack on which to create the balls and the radius and height

	X	Y	Arc Center X	Arc Center Y	CW		
1	20.000000	3805.000000					
2	25.000000	3805.000000					
3	45.000000	3825.000000					
4	45.000000	3915.000000					
5	85.000000	3925.000000					
6	75.000000	3925.000000					
7	55.000000	3935.000000					
8	55.000000	4065.000000					
9	50.000000	4080.000000					
10	25.000000	4080.000000					
11	1						
Add new vertex Add new vertex Below Below Cascel							



ANSYS Clipping the Design

• Slwave provides you with the option to cut out and view a particular region of the design, and ignore the rest of the geometry .

Clip

Design

- Edit > Clip Design
- Follow the 6 steps > Clip

Options F	For Clipping Design		×
1. Sele	ct dipping polygon shape		
• R	Rectangle		
© P	Polygon		000000
2. Drav	w dipping polygon using the mouse		8 3 8 8
(To clic	close polygon, return to the start p ck the right mouse button)	point, double-click or	
3. Cho	ose one of the following options fo	r clipping traces	
() ()	Cut traces crossing clipping polygon	boundary	
© 1	include all traces that overlap the d	lipping polygon	
© I	include only traces completely inside	e the clipping polygon	
4. Do y	ou want to ignore layer visibility du	uring the clip operation?	
() Y	es (Clip objects on all layers)		
© N	No (Invisible objects won't be clippe	:d)	
5. Do y	ou want to keep objects inside the	dipping polygon?	
() Y	(es		
O N	No (Reverse Cutting)		000000000
6. Click	the "Clip" button		
Cli	ip	Cancel	





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ANSYS Create a custom Reference Designator

- How to create your own reference designator inside SIwave UI ?
 - 1. Select via(s)/pad(s) of interest (those you wish to classify as belonging to a part/ref des.).
 - 2. Right-click and select "Properties" in the pop-up menu.
 - 3. In the "Via Properties" dialog set the following under the "Pin Info" section:
 - Type (either BGA or DIE)
 - Part name (any reasonable string)
 - Reference designator (any reasonable string)
 - Pin name (any reasonable string).

-This field is disabled if more than one pad/via has been selected; in this case, pin names are automatically generated ("1", "1", ...)

Via Properties	×
Top Layer	METAL-1
Bottom Layer	METAL-1
Rotation Angle	0 degrees
Mirrored?	No 🔻
Check layer(s) which the selected vias has antipads on As is (Uncheck to select layers)	METAL-1 METAL-2 METAL-3 METAL-4
Pin Info	
Туре	DIE
Layer	METAL-1
Part Name	Mycomponent 🔹
Ref. Designator	<u>U1</u> •
Pin Number	
Pin Name	(optional)
Delete	
ОК	Cancel



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3D Export

Fluid Dynamics

Structural Mechanics

Electromagnetics

Systems and Multiphysics

ANSYS How to do a 3D export?

1. Identify Power and Ground nets

Power/Ground Identif 👻 🏨 🛪
Search Exp:
Non Power/Ground Nets ABC BLT_DATA_P1 BLT_DATA_P2 BLT_DATA_P3 BLT_DATA_P4 BLT_DATA_R1 BLT_DATA_R3 BLT_DATA_R4 Power/Ground Nets GND P28VA VCC
Auto Identify

ANSYS How to do a 3D export?

2. Select Nets you wish to simulate





ANSYS What is a Plane Extent?

- Plane extents define the region that will be cutout when exporting to HFSS, Q3D Extractor, ANSYS Workbench, or Designer.
- Plane extents define the region that will be cutout for inclusion within an HFSS solve
- Plane extent operations
- Users must first define power and ground nets. This allows a cutout on those nets when trying to simulate signal nets.
 - Plane extents can be created automatically or manually
 - Automatic Plane Extents
 - Define the extent you want the cutout to extend beyond the signal traces (mm, um, mils, inches, ...)
 - Simple: Creates polygon cutout without Arcs
 - Precise: Creates polygon cutout with Arcs
 - Automatic Plane Extents to Terminals
 - Defines the extents to Wirebond, Solderball/Solderbump
 - Simple: Creates polygon cutout without Arcs
 - Precise: Creates polygon cutout with Arcs
 - Manual Plane Extents
 - User draws a plane extent in the layout editor window
 - Rectangle: Creates rectangular cutouts
 - Polygon: Creates polygon cutouts

ANSYS How to do a 3D export?

3D EXPORT PREVIEWS FOR

DIFFERENT PLANE EXTENTS





4. Go to Export > Preview Export (Clipped PWR/GND)

Image: Contraction of the contraction of







5. Export to HFSS, Q3D Extractor, Designer or ANSYS Workbench



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Validation check



Structural Mechanics

Electromagnetics

Systems and Multiphysics

ANSYS Slwave : Validation check

 Before you run an analysis on a model, it is very important that you first perform a validation check on the project. When you perform a validation check on a project, Slwave runs a check on all the setup details of the active project to verify that all the necessary steps have been completed and their parameters are reasonable.

Performing a Validation Check

- Tools > Validation Check.
- Self-Intersecting Polygons
 - Check for duplicating planes, intersecting edges, and check if voids intersect the plane boundaries.
- Disjoint Nets
 - Check if there are any nets that are not completely connected.
- DC-Shorted Errors
 - Check if any nets overlap.
- Identical/Overlapping Vias
 - Check if any vias are identical or overlap on the same nets.

aunch Validation Check	×
Check List	Select a simulation mode
Select All Unselect All	No Associated Simulation 🔹
Self-Intersecting Polygons	Minimum Area: 3100.01 mils^2
Disjoint Nets (Floating Nodes)	Cutouts that are smaller than this minimum area will be ignored during
DC-Short Errors	validation check.
✓ Identical/Overlapping Vias	This threshold can be changed in the Simulation -> Global Option window.
Bondwire Collisions	
✓ Illegal Bondwire Connections	Nets to be checked
V Misalignments	Some nets might not be included. Please refer the Simulation -> Global Option
Less Than Two Terminals	window.
	Number of cores to use: 4
ОК	Cancel

ANSYS Slwave : Validation check

Bondwire Collisions

- Check for duplicate or overlapping bondwires.

Illegal Connections of Bondwires

 Check if the inner radius of the via is more than the bondwire, or if the bondwire extends through the pad.

Misalignments

- Check for all misalignments, in the following cases:
 - to flag and auto-correct areas where the centerline of a trace is not contained within a plane.
 - if a trace overlaps with a plane, but the centerline of a trace doses not intersect with a plane.
 - if a trace overlaps with other trace, but the centerline of a trace does not intersect with the centerline of other trace.
 - if the boundary of a pad/via intersect with the boundary of a trace, but the center of a via/pad is not located on the centerline of a trace (in other words, the pad/via is not snapped to the centerline of a trace).
 - if the boundary of a plane intersect with the boundary of a pad/via, but the center of the pad/via is not contained in the boundary of the plane.

Unreferenced Trace Segments

- Check for traces with no reference plane above or below it.
- 87 © 2015 ANSYS, Inc. December 7, 2016

ANSYS Validation Check : Disjoint Nets

- Definition of a Net : A 'net' is a continues piece of metal. If two pieces of metal that are defined to be the same net are not DC shorted an error can occur .
- Disjoint Nets
 - Check if there are any nets that are not completely connected and highlights trouble with electrical connections.
 - A very common problem that arises sometimes is that piece of metal that have been added as shield are not physically connected to ground. These floating pieces of ground pour can actually serve as a radiating structure rather than provide effective shielding as the engineer was intending. Any floating pieces of metal should be connected through vias/additional metal or removed from layout.

To fix the disjoint nets

- Expand the Disjoint Nets error message



- The net GND has been identified as having disjoint geometry. Select this net from the nets listing
- Select Edit -> Nets -> Separate Disjoint Parts
- Click OK to the resultant message window.
- Scroll down the nets window and notice that additional nets were created from the disjoint pieces, net-1, net-2,....

ANSYS Validation check : Identical / Overlapping Vias

Identical/Overlapping Vias

• Check if any vias are identical or overlap on the same nets.



Identical/Overlapping Vias (Errors: 2, Warnings: 0)
 net "GND" (160.325000, 158.200000, 0.000000)
 net "SECURITE_GRILLES" (138.737500, 159.712500, 0.000000)



ANSYS Validation Check : Misalignments

Misalignments :





Edit > Nets

- Most of the Nets options are used to correct geometry that has been imported from a third-party layout tool. It is useful to first run a Validation Check (which will be described later in this section) to detect potential issues
- Merge
 - All Selected Nets
 - Merges all electrically connected nets that have been selected
 - Connected Nets
 - Merges all electrically connected nets in the set into a single net. It is not necessary to manually select these nets
- Check if Disjoint
 - Only checks the selected nets. The complete layout can be checked during the Validation Check
- Check for DC Short
 - Only checks the selected nets. The complete layout can be checked during the Validation Check
- Separate Disjoint Parts
 - If all parts of a net are not electrically connected this operation will allow these parts to be separated into different nets
- Misalignment
 - Select and View
 - No operation is performed, this is a visualization only
 - Correct
 - Slwave will try to correct the alignment. The misalignment will be detected in the Validation check. This occurs when a design has traces whose center lines are not connected to any planes or pads or the center lines of other traces
- Change Name

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Enter a new name







Original : The two pads look to be connected



For solver setup, the arcs are discretized and so they are not connected.



The auto fix can't separate the disjoint nets, but the validation check will point the separating locations of disjoint nets If a trace connecting two pads in the design is added manually, the net gets well-connected.

ANSYS Slwave GUI Controls – Results

Slwave Desktop : Results Window

- Users can define solve, and post-process multiple resonant mode, frequency, SYZ, etc., simulations
- Simulation results are no longer stored in the *.siw file but rather are stored in the *.siwaveresults subdirectory. Far-field results and network parameters are accessed from the desktop

Results

😑 쟁 SYZ

SYZ Sweep 1

SYZ Sweep 1MHz -> 1GHz Linear

🕶 🗜 🗙

- One quick integrated reporter with S,Y,Z tab
- Results can be exported to AEDT for post-processing
- Results can also be exported to NdE for causality/passivity check



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Circuit Element

Fluid Dynamics

Structural Mechanics

Electromagnetics

Systems and Multiphysics

ANSYS Slwave Circuit Element Parameters

Home > Circuit Element Parameters



- For local components (created and placed by you): you can see the part name, circuit elements and pins.
 - Next to each pin number, you can see the net to which it is attached.

Set Active or Set Not Active

A green check mark in front of the element shows that it is active and will be included in the analysis. A red cross shows that is inactive.



Circuit Element

Parameters



Direct import of passive component

Choosing appropriate model

- Three methodologies :
- Ideal resistor, inductors and capacitors
- TouchStone representation of Capacitors, Inductors, Resistors, and ICs
 - Vendor libraries of commonly used components (ESR, ESL included)
- Equation based RLC parasitics

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User defines parasitics at specific frequency

Set Capacitor Paramet	ters	x ·
Name:	C1	
Part Number:	C_custom 👻	
Capacitance:	1E-07	Farads
Parasitic Inductance:	1E-09	Henries
Parasitic Resistance:	0.05	Ohms
1	OK (Cancel
© 2015 ANSYS, Inc.	December 7. 2016	



Capacitor Library Browser...



ANSYS Examine Component Properties

 If you have a global part name selected: you can examine component properties, plot the component's impedance vs. frequency graph, or place a component either on the top layer or bottom layer



ANSYS Slwave : Component Management

To launch the Component Management dialog

• Tools > S-Parameter Model Assignment...

Local Part Name	Туре	Value	Size Est.	Manufacturer	Series	Part Name	Matched Value	Matched Size
CAPACITOR_CDR02	Capacitor	100.000000 nF	1808					
CAPACITOR_CDR04	Capacitor	100.000000 nF	1812					
CAPACITOR_CDR06	Capacitor	100.000000 nF	2525					
CAPACITOR_CSR13B	Capacitor	100.000000 nF	N/A					
CAPACITOR_CWR06-10V	Capacitor	47.000000 uF	3838					
NO_DEV_TYPE	Capacitor	100.000000 nF	1812					
NO_DEV_TYPE	Inductor	1.000000 nH	N/A					
Auto Match By Value Assign S-parameter Model]		Auto Clea	o Match By Name ar Model Assignme	ent		Import Pa Export Pa	rt Matching Fil rt Matching Fil
	1						Remove S	parameter Mor



• Matching can be done :

- Automatically by Matching part names or values
 - Click Auto Match By Value... or Auto Match By Name...
- Using a matching File :
 - Click Import Part Matching File ...

ANSYS Slwave : Part Matching File

In the Component Management dialog

Import Part Matching File

	S-parameter Component M	anagement	Dialog						X
	Local Part Name	Туре	Value	Size Est.	Manufacturer	Series	Part Name	Matched Value	Matched Size
	► CAPACITOR_CDR02	Capacitor	100.00000 nF	1808					
	CAPACITOR_CDR04	Capacitor	100.00000 nF	1812					
	CAPACITOR_CDR06	Capacitor	100.000000 nF	2525					
	CAPACITOR_CSR13B	Capacitor	100.00000 nF	N/A					
	CAPACITOR_CWR06-10V	Capacitor	47.00000 uF	3838					
		Capacitor	100.00000 nF	181Z					
	NO_DEV_TIFE	Inductor	1.000000111	N/A					
124									
Notepad++ - D:\newmap.pmap	Auto Match By Value]		Aut	o Match By Name			Import Par	t Matching File
File Edit Search View Format Language Settings Macro	Assign S-parameter Model]		Clea	ar Model Assignm	ent		Export Par	t Matching File
🗋 🖆 🖬 🗊 🗙 🔆 🐰 🖻 💼 여 여 👪 🏥 🍳 🍳	Import S-parameter Model]						Remove S-	parameter Model
newmap.pmap								ОК	Cancel
1 # <localpartname> <comptype> <manufactu:< td=""><td></td><td></td><td></td><td></td><td>_</td><td></td><td></td><td></td><td>/</td></manufactu:<></comptype></localpartname>					_				/
2 2113945L49 Capacitors Murata GRM18 GRM	188R71H103KA01								
3 2113945L43 Capacitors Murata GRM18 GRM	188R71H562KA01								
4 2113944C85 Capacitors Murata GRM18 GRM	1885C1H510JA01								
5 2113944A80 Capacitors Murata GRM15 GRM	1555C1H200JZ01								
6 2113945L35 Capacitors Murata GRM18 GRM	188R71H272KA01								
7 2113946E02 Capacitors Kemet C0805C C08	05C105K4RAC								
8 4887559V16 Capacitors AVX NiobiumOxide	NOJ series NOJA106K0	06R							
9 2414032B69 Ind Coilcraft 1008CS 1008CS	-122								
11									

ANSYS Slwave : Part mapping file

×

Part Matching from Part Number

The vendor part number in the BOM may not be an exact match to a value in the library.

Couldn't find global part name with Manufacturer Name "TDK", Series Name "C1005" and Part Name "C1005X7R1E103K(M)". Please select a closely matching part name from the list below

Part Names

Select Part Name





Wide-band scatteringparameter models are automatically assigned from the SIwave library.

ANSYS Slwave : part mapping file

* Syntax for specifying parts:

<part name> <type> <val> <pin order>

which gives little clue as to supported strings for the <type>, <val>, & < pin order> fields

There is a component mapping file that has the format like this: # <partname> <ParasiticCap> <ParasiticInd> <ParasiticRes> R_PAK_0402X4-15,5%,31.25MW,N/AA Res 1.500000e+01 R_0603-750,1%,1/16W,N/A-1%,1/1A Res 7.500000e+02 R_0603-75,1%,1/16W,N/A-1%,1/16A Res 7.500000e+01 R_0603-7.5K,5%,1/16W,N/A-1/16WA Res 7.500000e+03

Which can be exported through File > Export > Component Mapping File

Then there is a PMAP file which has the format:

<CustomerPartNumber> <Type> <Vendor> <Family> <PartNumber>

ANSYS Example : part mapping file

• So if the customer has a part number called CUST203204932 which is a 0201 cap that would map to an AVX capacitor family 0201 part number <0201YA390JA>:



- Then the Customer.PMAP file would be a text file that would have then entry:
 - CUST203204932 Capacitors AVX 0201 0201YA390JA
- This file would perform the mapping under the Tools à Component Database à Part Matching File

ANSYS Slwave : Port Assignment



ANSYS Slwave : Manually draw a Port

- Top-Down view must be activated
- Circuit Elements > Add Port
- Click 2 times to define the positive and negative pin.
- Define the Positive and Negative Terminals by choosing a layer
- A port can be placed everywhere

ayer	Net	Layer	Net
SURFACE	CLK_1K	SURFACE	VCC
L2	GND	🗖 L2	GND
L3		🗖 L3	
L4		🗖 L4	
L5		🗖 L5	
L6	P28VA	📕 L6	P28VA
L7	VCC	🗖 L7	VCC
BASE	CLK_1K	BASE	

x Port Properties CLK_1K Name: Reference Impedance: 50 Ohms Positive Terminal Net: CLK_1K Negative Terminal Net: GND Positive Terminal Pin: (26)U17 Reference Terminal not connected to Pin or Pingroup Port (Active) Name: CLK 1K Zref: 50ohms + Net: CLK 1K - Net: GND





Slwave : Generate on selected net **ANSYS**[®]

- Generate the port on the selected net
 - Select the net(s)
 - Tools > Generate on Selected net...

Check Nets to Process	Check Pins to Process on Net SC_PARA_DATA0 (Click on the Green Tick / Red Cross mark to deactivate / activate the ports on the respective pins)	
SC_COMPLETE SC_CTL SC_EN_N SC_ERROR SC_PARA_DATA0 SC_PARA_DATA1 SC_PARA_DATA2 SC_PARA_DATA2 SC_PARA_DATA3 SC_PARA_DATA5 SC_PARA_DATA5 SC_PARA_DATA6 SC_PARA_DATA6	Pin Name Ref. Des. Part Driver/Receiver ✓ 16 U49 74ACT299_SOIC ✓ 18 U34 PAL22V10_SMSOCKE	
Port Options Ref. Impedance: 50.0 ohms	Ref. Net: GND Ref. Type: Pin Pin Group	Port (Ac Name: C Zref: 500



ANSYS Slwave : Generate on Component

- Generate port on component
 - Select a component
 - Tools > Generate on Component...
 - Define Positive and Reference terminal



Circuit Element Generation Dialog						23
Positive Terminal Component		Reference T	erminal Compone	ent		
Part Name: 74ACT299_SOIC		Part Name:	[74ACT299_SO	IC		_
Ref Des: U35	•	Ref Des:	U35			
		V Same as F	Positive Terminal			
Circuit Element Positive Terminal	Circuit Element Reference	Terminal		Circuit Elements		
				Capacitors		_
ST_CNTL_SR0	ST_CNTL_SR0			···· Current Sources		
ST_CNTL_SR1	ST_CNTL_SR1			Inductors		
. ST_DATA4	ST_DATA4			Resistors		
	SI_DATA5 SI_DATA6			Ports		
				Voltage Brober		
				Woltage Sources		
	UN14AC257209PY	0		Terminals		
UN14AC257209PY0	UN14ACT299220P	DS70				
UN14ACT299220PDS70	UN14ACT299220P	MR0				
UN14ACT299220PMR0	UN14ACT299220P	Q70				
UN14ACT299220PQ70						
i ·· VCC						
	Expand Collapse	Find Pin at Lo	cation			
	Use nearest pin as re	ference pin				
		· · ·				
	Group pins within the	reference distan	ice			
	Circuit Element Type					
	Capacitor	Port				
		Current	Source			
Expand Collapse Find Pin at Location	Decistor	 Valtage I 	Source			
Reg Expression syntax {Net name}:{Pin name}	C Resistor	 Voltage : 	Deska			
	S-Param Cir Elem	voltage i	robe	Delete	C	
ineg exμ.	I erminal			Delete	Edit	
	Naming Convention	Create		OK	Can	cel



ANSYS Slwave : Create Differential Pairs

- Make sure that the Differential workspace is checked :
 - Visibility > Workspaces > Differential Nets
- This area allows you to define, search, sort and remove the differential pairs.
- An Auto Identify feature find differential pairs using the positive and neagtive net suffix.
 - Define + & net suffix
 - Auto Identify

Auto Identify Diffe	erential Pairs		×
Differential P BLT_DATA1 BLT_DATA2 BLT_DATA3 BLT_DATA4 TSD	air Name	Positive Net BLT_DATA_P1 BLT_DATA_P2 BLT_DATA_P3 BLT_DATA_P4 TSD_P	Negative Net BLT_DATA_R1 BLT_DATA_R2 BLT_DATA_R3 BLT_DATA_R4 TSD_R
Auto Identify S + Net Suffix: - Net Suffix:	_P _R	 Append to grid content Replace grid contents 	Delete Selected Row(s)
Auto Identify OK Cancel			
ANSYS Slwave : Create Extented Nets (E Net)

- Make sure that the Enet workspace is checked :
 - Visibility > Workspaces > Extended Net
- This area allows you to define, search, sort and remove the Enets. Most extended nets in real usage consist of only 2 nets with names like "NET1" and "NET1_R" connected by a resistor.
- An Auto Identify feature find Extended net using a keyword (i.e. the net name differentiator) should be just "_R"
 Auto Identify Extended Nets

Auto Identify Extended Nets				×
1	-			
Extended Net Name	Nets			
HSSL_EXTD	HSSL_R, HSSL	-		
Auto Identify Settings			Delete Selected Row(•
Net Name Differentiator:		Append to grid contents		
		Replace grid contents		
		0		
Auto Id	entify			
			OK Ca	ncel

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Classic questions about Port Settings

Fluid Dynamics

Structural Mechanics

Electromagnetics

Systems and Multiphysics

ANSYS Classic questions about Port Settings

- What if a port in Slwave does not have a connection to a reference plane, but is connected between two signal locations? Does this invalidate the results?
- S-parameter models generally consist of ports referenced to ground.
- In DesignerSI, the S-parameter symbol is often in is an "implied reference to ground" format.

ANSYS A Simple Example

- Consider a 2-inch long trace over a reference plane.
 - Ports P1 and P2 between the trace and plane at each end



Model in AEDT, with a source at P1 and P2 shorted to ground:





• Source drives a 100ps edge





ANSYS Now Split the Trace In Two...

- Now two traces of roughly 1 inch in length
- Ports to ground at all trace ends





Connect a series inductor between P2 and P3

ANSYS Series Inductor Results

- Inductor causes small positive reflection in the middle of the waveform
- **Results still perfectly intuitive**





•

ANSYS Now Place Just One Port In the Middle

• Same pair of 1-inch traces, but now place a single port P2 across the gap between them. P2 positive P2 reference

P2

No connection to reference plane at P2





In the circuit schematic, we only have one pin. How do we connect the series inductor? If we connect it between the P2

terminal and circuit ground, will that short out the second trace?

P1

ANSYS No. Results Are The Same

- Voltage between node P2 and circuit ground corresponds to voltage across the positive and reference terminals of the Slwave port
- Circuit ground and physical reference plane are completely different things



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Slwave Solvers

Fluid Dynamics

Structural Mechanics

Electromagnetics

Systems and Multiphysics

ANSYS Slwave Solver Technology

Slwave solver components:





Same FEM technology as HFSS, but for layered structures, i.e. 2D nonuniform mesh

$$\mathbf{E} = \hat{\mathbf{z}} E_z(x, y)$$

$$\mathbf{H} = \hat{\mathbf{x}}H_x(x, y) + \hat{\mathbf{y}}H_y(x, y)$$

E





Separation between the metal planes is much less than the wavelength

2D restriction offers a major speed and memory advantage

ANSYS 2-D Full-wave FEM continued

• The Maxwell's equations can be reduced to a wave equation in terms of the voltage difference between planes.

$$\frac{1}{R+j\omega L}\nabla^2 V(x,y) - (G+j\omega C)V(x,y) = I$$

The pre-processor identifies where the assumption is valid

ANSYS Slwave - Hybrid Solver

Slwave is a Hybrid Solver

- The pre-processor validates the layout, identifies and categorizes structures, assembles matrix and passes to sparse matrix solver.
- When is $\mathbf{E} = \hat{\mathbf{z}} E_z(x, y)$ not valid?
 - Traces
 - Trace-plane coupling
 - Via transitions
 - Plane edges
 - Bondwires, balls, bumps
 - Coaxial probes



EXERCISES Correct Handling of All Plane Effects and Dielectric Losses Frequency-dependent plane impedance $\int_{R_{dc}}^{\log R(f)} \int_{R_{ac}}^{\log f(f)} \int_{L_{dc}}^{L(f)} \int_{L_{dc}}^{L($

Correct Handling of Dielectric Losses

- Loss tangent and permittivity vary with frequency in a coordinated way
- Djordjević-Sarkar model
 - Satisfies causality laws -> physically realistic behavior

ANSYS MoM Modeling of Traces

2D MoM RLCG trace extraction

- Generalized multilayer extraction
 - Transmission lines
 - CPW
 - Split planes
- Non-uniform material stackups
- Trapezoidal and hexagonal cross-sections
- High accuracy and speed
 - Adaptive meshing of the trace cross-sections
 - Fast frequency sweep acceleration
- Multithreaded solve capability with perfect scaling

• Automatic coupling based on dB threshold

ANSYS Slwave Modeling of Traces

• Define Trace Cross Section by choosing the appropriate shape by layer:

Edit > Trace Cross Section...

Rectangle

Rectangular, Trapezoidal and hexagonal

Trapezoid

x x Trace Cross Section Shape Editor Trace Cross Section Shape Editor Layer: SURFACE • Laver: SURFACE • Shape: Rectangle -Shape: Trapezoid Ŧ W1 Etching Style Etching Style Over Etch Over Etch O Under Etch O Under Etch Formula (Trapezoid Only) Formula (Trapezoid Only) W1 = Width * N/A Width W1 = Width * 0.85 W1 = Width - N/A * Thickness W1 = Width - 0.85 * Thickness Set Ratios Set Ratios Set Absolute Values For Etching Set Absolute Values For Etching Top: Top: <u>n</u>-W1: W1: 100 % 85 % W2: W2: Bottom: Bottom: 100 % 85 % Slide Both Simultaneously Slide Both Simultaneously OK Cancel OK Cancel







Additional Solver Capabilities...

Vias

• Quasi-static FEM. Recognize repeated structures and solve only once.

Plane edges: edge-edge coupling

• 2D-MoM. Similar to transmission line modeling

Plane edge to trace coupling

• 2D-MoM

Low frequency plane-plane coupling

Passive components (RLC or s-parameters)

Bondwires & Balls and bumps

Fast quasi-static 3D MoM (or Boundary Element Method)

Efficient, accurate full-wave analysis of complex PCB's is possible due to

- Sophisticated "pre-processing" that properly recognizes and categorizes 3D features.
- Multiple EM solvers working in combination.
- Advanced Numerics (Matrix solver)

ANSYS Slwave Solver Components

Further models for improved accuracy:

• Fringe fields: correction for thin planes (very critical for inductance!).



Smart coupling detection: coupling between traces/plane edges and via coupling.



 Coplanes, split planes and thin planes: plane – plane and trace plane coupling.



ANSYS Slwave - Via Modeling

New VIA library - IBM Benchmark Examples

Taken From: Selli, G., et al, "Developing a 'Physical' Model for Vias," DesignCon 2007

Single Through Via -- Measured SIWAVE v4.0 -10 -15 S21(dB) -20 -25 -30

Single Through Via + Ground Via





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10

15

20

Frequency (GHz)

25

30

35

40

5

-35

-40<u></u>



Board level - Via Stub effect





A 3D method of moments solver is used to extract the RLC parasitics, including self and mutual terms







- RLC components can be modeled as:
 - Lumped Element
 - Touchstone file



Ferrites included as a Touchstone model



Component attachment accurately modeled from pad dimensions

Realize Your Product Promise™



Simulation Options

Fluid Dynamics

Structural Mechanics

Electromagnetics

Systems and Multiphysics



Simulations > Options...

	a							
	SIwave Options	Lance allocation						
Optimum speed	SI/PI SI/PI Advanced DC	DC Advanced Multiproce	essing Net Processing					
PI simulation	Coupling	Plane Void Meshing						
	Coplane				57			
Optimum speed	Intra-plane	Siwave Options						
	Split-plane	SI/PI SI/PI Advanced	DC DC Advanced Multip	processing Net Processing				
Custom (as la stine strine st	Cavity field							
Custom (selecting this opt	Cross-talk		Π					
	threshold: -34 dB		Slwave Options		X			
		Optimum speed						
	Trace return current dist		SI/PI SI/PI Advanced	DC DC Advanced Multi	processing Net Processing			
	Include Voltage/Current	Custom (select	Initial Mesh Max. Edge Ler	ngth: 455mil	Perform Adaptive Mesh Refinement			
	Introduce infinite ground	V Plot Current De	Mesh Bondwires		Adaptive Mesh Refinement Parameters			
	Perform ERC during simi	Circuit element co	- Bondwire Discretizatio	SIwave Options		×		
	Exclude non-functional p	Exclude non-functional p		Approximate cylindric SI/PI SI/PI Advanced DC DC Advanced Multiprocessing Net Processing				
	(non-runcuonal paus are			Multiprocessing				
			Mesh Vias	Number of cores to	4			
			Via Discretization					
			Approximate cylindrica	Use HPC licensing	Stwave Options			
				May	Styri Styri Advanced DC DC Advanced Multiprocessing			
					Use current net selection for simulation			
				Simulation server	Auto select nets for simulation			
	L				✓ Ignore nets named "DUMMY" or "Unused" during Simulation			
					Additional Nets to Include in Simulation			
					SIwave ALWAYS includes nets containing at least one plane.			
					During frequency sweeps, nets to which sources or probes are attached			
					are automatically included. During 512 barameter sweeps, nets to which			
					ports are attached are automatically included.			
					ports are attached are automatically included. Select any additional nets to include in the simulation from the following list:			
					are automatically included: Journal of the photometer sweeps, nets to writer ports are attached and automatically included. Select any additional nets to include in the simulation from the following list: 			
					are automatically included: Journal of a parameter sweeps, nets to winch ports are attached are automatically included. Select any additional nets to include in the simulation from the following list: 			
					are automating included: Journg Siz parameter sweeps, nets to wind ports are attached are automatically included. Select any additional nets to include in the simulation from the following list: DUMMY NETO NETO NETO NETO NETO NETO NETO			
					are automating included. Unity of a parameter sweeps, nets to which ports are attached as automatically included. Select any additional nets to include in the simulation from the following IST UNINY UCTO NETO NETO NETO Part_neg part_neg part_neg part_neg			



Use FEM Discretization

Mesh Refinement. This parameter controls how the finite element mesh used in Slwave is generated. You can select from the following options:

- Automatic: This options automatically picks the suitable mesh refinement frequency. It is dependent on the drawing size, the number of modes, and/or the maximum sweep frequency. This is the recommended option.
- **Frequency:** This option lets you control the mesh size and is based on the effective wavelength of the specified frequency.





Automatic : Fmax = 10GHz

ANSYS 3D return current distribution

• 3D return current distribution check box if you want to accurately model the change of the characteristic impedance of transmission lines caused by a discontinuous ground plane. Instead of injecting the return current of a trace into a single point on the ground plane, the return current for a high impedance trace is now spread out.



- The trace return current is not distributed when all traces attached to a node have a characteristic impedance of less than 75 ohms, or if the difference between two connected traces is less than 25 ohms.
 - Not really necessary for PI related simulations.
 - For SI analysis it is quite useful and improves accuracy.
 - Slow down the simulation noticeably. RAM is slightly increase by more matrix entries and some other overhead.

ANSYS Coupling Options in Slwave

Solver Coupling Options

- By default, all coupling options are disabled. Please check the box Custom in the SI/PI tab to enable them.
- Co-Plane
- Intra-Plane
- Split-Plane
- Cavity Field
- Trace

SIwave Options				
SI/PI Advanced DC	DC Advanced Multiprocessing Net Processing			
Coupling	Plane Void Meshing			
Coplane	Do not mesh any voids less 2mm2			
Intra-plane				
🗸 Split-plane	Restore Default			
Cavity field				
✓ Trace	Mesh Refinement			
Cross-talk threshold: <mark>-34</mark> dB	Automatic Frequency			
Trace return current distribution				
Include Voltage/Current Source Connections/Parasitics in Resonance/SYZ Simulations				
Introduce infinite ground plane 0mm below bottom layer in				
Perform ERC during simulation setup (abort when an electrical short or floating geometry is detected				
Exclude non-functional pads from resonant mode, frequency sweep and SYZ simulations (non-functional pads are always excluded from DC IR drop simulations)				
	OK Cancel			



Case 1 – 1 trace, 1 plane

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ANSYS Coupling – Split Plane

With and without Split Plane Coupling

- With all the options enabled, SIwave calculates coupling between trace2 and GND_left
- When Split Plane is disabled there is no coupling between the two



ANSYS Coupling – Split Plane – Two Cases

With and without Split Plane Coupling

- With all the options enabled, SIwave calculates coupling between trace2 and GND_left
- When Split Plane is disabled there is no coupling between the trace2 and GND_left





Case 2 – 1 trace, 2 planes

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ANSYS Coupling – Split Plane

With and without Split Plane Coupling

- With all the options enabled, SIwave calculates all coupling including coupling between narrow planes like plane_2 and traces like trace_1
- When Split Plane Coupling is disabled, there is no direct coupling between trace_1 and plane_2



ANSYS Coupling – Split Plane

With and Without Split Plane Coupling

- Only coupling between the trace and GND plane are significant



ANSYS Coupling – Coplane

With and without Coplane Coupling

- When Split Plane Coupling is disabled, there is no direct coupling between trace_1 and plane_2
- If Coplane is also disabled, no coupling is computed between traces and planes



ANSYS Coupling – Coplane

With and Without Coplane Coupling

Only coupling between the planes, plane_2 and GND are reported when Coplane is disabled




Case 3 – 2 traces, 1 plane

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With and without Trace Coupling



Split Plane and Coplane Two Trace Model

- For the Two Trace Model the results are the same as the Split Plane Enabled
- Disabling the Coplane excludes the coupling between each trace and the ground



NNSYS®



With and Without Trace Coupling

Freq [GHz]	db(S(GND,trace_1)) SYZ Sweep all options two trace model	db(S(GND,trace_2)) SYZ Sweep all options two trace model	SYZ Sweep all options two trace model
0.001000	-80.094041	-79.939533	-80.268550
0.010998	-81.500037	-74.406131	-63.452760
0.020996	-79.837461	-69.370202	-58.019106
0.030994	-77.104160	-66.019871	-54.757956
0.040992	-74.213273	-63.519997	-52.439362
0.050990	-71.614311	-61.531155	-50.645301
0.060988	-70.062135	-60.043304	-49.143095
0.070986	-68.753971	-58.786333	-47.869037
0.080984	-67.626534	-57.699034	-46.762601
0.090982	-66.637847	-56.741630	-45.784876
0.100980	-65.758885	-55.886934	-44.909291
0.110978	-64.968820	-55.115593	-44.116836
0.120976	-64.252223	-54.413357	-43.393409
0.130974	-63.597366	-53.769421	-42.728244
0.140972	-62.995129	-53.175396	-42.112926
0.150970	-62.438292	-52.624630	-41.540749
0.160968	-61.921043	-52.111755	-41.006282
0.170966	-61.438639	-51.632369	-40.505065
0.180964	-60.987161	-51.182820	-40.033393
0.190962	-60.563334	-50.760038	-39.588152
0.200960	-60.164395	-50.361418	-39.166703
0.210958	-59.787992	-49.984729	-38.766791
0.220956	-59.432106	-49.628047	-38.386472
0.230954	-59.094988	-49.289698	-38.024060
0.240952	-58.775118	-48.968215	-37.678086
0.250950	-58.471159	-48.662309	-37.347257
0.260948	-58.181934	-48.370838	-37.030433
0.270946	-57.906399	-48.092784	-36.726604
0.280944	-57.643621	-47.827237	-36.434869
0.290942	-57.392766	-47.573381	-36.154421
0.300940	-57.153082	-47.330479	-35.884537
0.310938	-56.923888	-47.097862	-35.624563
0.320936	-56.704568	-46.874923	-35.373909
0.330934	-56.494560	-46.661110	-35.132038
0.340932	-56.293350	-46.455915	-34.898460
0.350930	-56.100465	-46.258873	-34.672731
0.360928	-55.915472	-46.069557	-34.454441
0.370926	-55.737971	-45.887570	-34.243215
0.380924	-55.567591	-45.712547	-34.038708
0.390922	-55.403988	-45.544148	-33.840601
0.400920	-55.246843	-45.382057	-33.648601
0.410918	-55.095858	-45.225980	-33.462434
0.420916	-54.950755	-45.075642	-33.281847
0.430914	-54.811272	-44.930786	-33.106607
0.440912	-54.677165	-44.791169	-32.936492
0.450910	-54.548206	-44.656566	-32.771301
0.460908	-54.424177	-44.526762	-32.610841
0.470906	-54.304875	-44.401557	-32.454934
0.480904	-54.190106	-44.280761	-32.303413
0.490902	-54.079690	-44.164193	-32.156122
			1

Freq [GHz]	db(S(GND,trace_1)) SYZ Sweep no trace two trace model	db(S(GND,trace_2)) SYZ Sweep no trace two trace model	db(S(trace_1,trace_2)) SYZ Sweep no trace two trace model
0.001000	-inf	-inf	-inf
0.010998	-inf	-inf	-inf
0.020996	-inf	-inf	-inf
0.030994	-inf	-inf	-inf
0.040992	-inf	-inf	-inf
0.050990	-inf	-inf	-inf
0.060988	-inf	-inf	-inf
0.070986	-inf	-inf	-inf
0.080984	-inf	-inf	-inf
0.090982	-inf	-inf	-inf
0.100980	-inf	-inf	-inf
0.110978	-inf	-inf	-inf
0.120976	-inf	-inf	-inf
0.130974	-inf	-inf	-inf
0.140972	-inf	-inf	-inf
0.150970	-inf	-inf	-inf
0.160968	-inf	-inf	-inf
0.170966	-inf	-inf	-inf
0.180964	-inf	-inf	-inf
0.190962	-inf	-inf	-inf
0.200960	-inf	-inf	-inf
0.210958	-inf	-inf	-inf
0.220956	-inf	-inf	-inf
0.230954	-inf	-inf	-inf
0.240952	-inf	-inf	-inf
0.250950	-inf	-inf	-inf
0.260948	-inf	-inf	-inf
0.270946	-inf	-inf	-inf
0.280944	-inf	-inf	-inf
0.290942	-inf	-inf	-inf
0.300940	-inf	-inf	-inf
0.310938	-inf	-inf	-inf
0.320936	-inf	-inf	-inf
0.330934	-inf	-inf	-inf
0.340932	-inf	-inf	-inf
0.350930	-inf	-inf	-inf
0.360928	-inf	-inf	-inf
0.370926	-inf	-inf	-int
0.380924	-inf	-inf	-inf
0.390922	-inf	-inf	-inf
0.400920	-inf	-inf	-inf
0.410918	-inf	-inf	-int
0.420916	-inf	-inf	-int
0.430914	-inf	-inf	-int
0.440912	-inf	-inf	-inf
0.450910	-inf	-inf	-int
0.460908	-inf	-inf	-int
0.470906	-INT	-INT	-INT
0.480904	-INT	-INT	-INT
0.490902	-INT	-INT	-int



With and without Cavity Field Coupling

- Cavity Field coupling models the effect of fringe field between cavities
- Two cavities are represented by the following stackup

C	Name	Туре
	DIELECTRIC-1	DIELECTRIC
	Тор	METAL
	DIELECTRIC-2	DIELECTRIC
	Middle	METAL
	DIELECTRIC-3	DIELECTRIC
	Bottom	METAL
	DIELECTRIC-4	DIELECTRIC
	Middle2	METAL
	DIELECTRIC-5	DIELECTRIC
	Bottom2	METAL







With and Without Trace Coupling

- Coupling between the Top Layer, top cavity and bottom layer, bottom cavity





Recommended Slwave Solution Settings

Fluid Dynamics

Structural Mechanics

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- Automatic void detection preferred
- Enable coupling except intraplane coupling
- Disable trace return current distribution
- Do not select additional nets to include in the simulation
- Use Trace return current distribution when signal traces switch layers frequently (slowdown)

Slwave Options	Slwave Options
SI/PI SI/PI Advanced DC DC Advanced Multiprocessing Net Processing	SI/PI SI/PI Advanced DC DC Advanced Multiprocessing Net Processing
SI simulation Optimum speed Balanced Optimum accuracy	Coupling Plane Void Meshing Coplane Do not mesh any voids less 2mmiz Intra-plane Restore Default
PI simulation Optimum speed Balanced Optimum accuracy	Image: Constraint of the second se
Custom (selecting this option allows you to configure advanced solver settings)	Trace return current distribution Include Voltage/Current Source Connections/Parasitics in Resonance/SYZ Simulations Introduce infinite ground plane Omm below bottom layer in Perform ERC during simulation setup (abort when an electrical short or floating geometry is detected V Exclude non-functional pads from resonant mode, frequency sweep and SYZ simulations (non-functional pads are always excluded from DC IR drop simulations)





- Explicitly set the Plane Void Meshing for a low bandwidth sweep up to a few GHz
- Enable coupling except intraplane coupling
- Disable trace return current distribution
- Select additional nets to include in the simulation if Sparameters models are attached to components
- Use Trace return current distribution when signal traces switch layers frequently (slowdown)







- Automatic void detection preferred
- Disable all coupling
- Disable trace return current distribution
- Do not select additional nets to include in the simulation
- Use do not Explicitly Mesh voids
 < 0mm² when PI solutions
 contain Hatched Planes
 (Slowdown)
- Use Intra-plane Coupling when DC solution accuracy is extremely important (RAM increase & slowdown)







- Select a few frequency points only (harmonics)
- Select an observation layer at least 3mm away from the PCB

Compute Near I	Field				x			
Simulation name: Near Field Sim 1 Excitations Use sources defined in project Use sources defined in external file Browse								
✓ Interpolate spectrum at missing frequency points Frequency Range Setup								
	Start Freq	Stop Freq	Num. Points	Distribution				
1 10	00kHz	2GHz	100	00 Linear				
Add /	Above Ad	d Below	elete Selectio	n Preview				
+x offset:	3	mm	Min	Adapt Passes: 1				
-x offset:	3	mm	Max	Adapt Passes: 10				
+y offset:	3	mm	Triangle	s to Add / Pass: 20	%			
-y offset:	3	mm	Global E	Error Tolerance: 3	%			
+z offset:	3	mm	Maxir	num Edge Length	_			
-z offset:	3	mm		Automatically determined	н			
Other solver of	options	Save	Settings	Launch	ose			

ANSYS Slwave Setup Guide for SYZ simulation

- Use the Djordjevic-Sarkar model
 - Slwave "standard" dielectrics use Djordjevic-Sarkar by default
- Frequency Sweep
 - Include DC point
 - Decade sweep from low frequency to around 1GHz
 - Linear spaced sweep for 1GHz to highest frequency
 - Set highest frequency to a minimum .35/tr where tr is the rise time
 - Error Tolerance : Set to .001 (default is .005)
- Impedances
 - Set power plane solution impedances to 1 ohm
 - Set transmission line solution impedances to 50 ohm
- Exporting s-parameter files
 - Renormalize to 50 ohm or 1 ohm according to application.



Signal Integrity simulation - Basics

Fluid Dynamics

Structural Mechanics

Electromagnetics

Systems and Multiphysics

ANSYS Signal Integrity Analysis

- Slwave can be used to extract models that accurately model return path, parasitics and all relevant coupling .
- Models can be in the form of a Touchstone file (v1.0 and v2.0), FWS SPICE subcircuit, lumped RLGC and others, and can be used for any time/frequency analysis
- SSO
 - Verify signaling with non-ideal power delivery to drivers
- Eye diagrams
 - Verify signal is clean enough for proper detection
- Cross-talk
 - Verify neighbors do not cause excessive noise
- Within SIwave environment, some analyses include Insertion/Return loss, Coupling, TDR and TDT, you can view frequency domain data and time domain data using an IFFT

ANSYS SI Analysis Setup

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34-10 311

To Perform a circuit extraction or SI analysis, place ports in desired location

Ports are similar to probes in lab measurements

34-10 294

ANSYS S-,Y-, Z- Analysis

- To extract S, Y and Z matrix for the predefined ports :
 - Simulation > Compute S-,Y-,Z-parameters
 - Enter the value for Start Frequency.
 - Include DC point
 - •Decade sweep from low frequency to around 1GHz
 - •Linear spaced sweep for 1GHz to highest frequency
 - •Set highest frequency to a minimum .35/tr where tr is the rise time
 - Specify the Number of Solution Points.
 - Select the method for distributing points
 - Choose the sweep Selection
 - Discrete sweep
 - Interpolating sweep

C	ompu	ite S	SYZ-paramete	rs			X			
	Swee	≥p	Sensitivity Di	stributed Analy	sis (HPC)					
		Simu	lation name:	SYZ Swe	eep 1		•			
		V (Compute exact	DC point						
	ſ	Freq	quency Range S	etup						
			Start Freq	Stop Freq	Num. Points / Step Size	Distribution				
		1	1Hz	1GHz	20	By Decade				
		2	1GHz	5GHz	100	Linear				
	Add Above Add Below Delete Selection Preview									
	Sweep Selection Image: Discrete Sweep Relative error for S: Image: Discrete Sweep Relative error for S: Image: Discrete Sweep Relative error for S: Image: Discrete Sweep Image									
	Export Touchstone® file after simulation completes File path: E:\SVN_Training\SIwave\input_files\WS01_2\siwave_ Browse									
					Save Settings	Launch	Close			

ANSYS Frequency Sweep Selection box

Discrete Sweep:

• All frequency points in the list are solved. Look at the Frequency List Preview.

Interpolating Sweep:

- Following an Error tolerance, an interpolating sweep estimates a frequency response for an entire frequency range by solving at a relatively small number of frequency points within that range. Between the actual solution frequencies, the frequency response is obtained by rational interpolation. Slwave adaptively chooses the frequency points at which it computes the field solution. After a new frequency point is solved, a new interpolating fit is generated. This is compared to the interpolant from the previous step, and the maximum difference between the two is determined. If the difference exceeds the requested tolerance, then a new frequency point is chosen for a solution. The interpolating sweep is complete when the difference between successive interpolants is less than the error tolerance criterion.
- Optionally, to save these settings and use them for subsequent simulations, click the Save Settings button



Close



• During simulation, in the Process Monitor workspace, you can follow the simulation progress. profile, monitoring the real time, CPU time, memory requirements and view the matrix informations.



- When the simulation is done, the profile is available with real time, CPU time, memory requirements and view the matrix informations.
- Results > Analysis Name > View profile

commenced	wave_ng 5.0.0 on host LyORI	D (Built: No FERNAND7L at	Won Feb 0	04:34:46) 7 22:18:26 2011	
Command	Real	Cpu Time	Memory		Ī
geomproc solve_setup	00:00:02	00:00:01	12276K 57780K	2040 triangle 1 project	
inished on LYC	RFERNAND7L a	t 02/07/2011	22:18:30		-
SIV	ave 5.0.0 No	9 2010 at	11:47:27	beginning	
	Beal		Memory		
Command	Time	Time	Michiol y	Number of Elements	
geomproc	00:00:00	00:00:00	11128K	2040 triangle	
via extract	00:00:00	00:00:00	23524K	/ XSECLIONS	
bsm_adapt	00:00:04	00:00:03	36868K	18246 triangles	
DRS_2p	00:00:00	00:00:00	73280K	21162 matrix	
SIwave	00:00:02	00:00:01	73280K	21162 matr1x	1
inished on LYC	RFERNAND7L a	t 02/07/2011	22:18:37		-
C Solution Pro	file:				
модите	Real lime	CPU Time	Memory	Size	





Realize Your Product Promise™



Signal Net Analyzer



Structural Mechanics

Electromagnetics

Systems and Multiphysics

ANSYS Signal Net Analyzer (SNA) in Slwave



ANSYS Signal Net Analyzer – Impedance Delay

- The Signal Net Analyzer gives you the ability to get a quick idea of characteristic impedance and also to rapidly generate transient voltage waveforms (using HSPICE or Nexxim simulations) of pin-to-pin signal propagation. The Signal Net Analyzer generates an impedance delay plot for each trace path selected. It also works for differential pairs.
- Tools > Signal Net Analyzer



ANSYS Signal Net Analyzer – Transient Response



Realize Your Product Promise™



Slwizard

Fluid Dynamics

Structural Mechanics

Electromagnetics

Systems and Multiphysics



Simulation > Slwizard...

Automates the creation of

- Pin groups containing power/ground pins
- Ports on both signal and power nets
- SYZ data (DC to fstop, based on signal TR/TF)
- FWS deck
- AEDT schematic
- Time domain voltage waveforms at drivers, receivers and power supply pins of all buffers
- Eye diagrams









Buffer Assignment



Set "Class" to IBIS

Correct IBIS buffer model assigned to all component pins

	IC		
	Part Number	BGA80P9X15-90	
	Ref. Des	U11	
	Default Buffer Models		
	Class	IBIS	
	Туре	Driver (Active)	
	Corner	Typical	
	Component	MT47H16M16BG_CLP-3_25	
Ξ	MT47H16M16BG_CLP-3_25		
	Manufacturer	Micron Technology, Inc.	
	R_pkg (typ.)	56.5m	
	L_pkg (typ.)	1.96nH	
	C_pkg (typ.)	0.27pF	
	Model	CLKIN_800	
Ξ	Pins		
	DDR-A0:M8	CLKIN_800 (Input with clamps)	
	DDR-A1:M3	GND	
	DDR-A2:M7	GND	
	DDR-A3:N2	IN_800 (Input with clamps)	
	DDR-A4:N8	CLKIN_800 (Input with clamps)	
	DDR-A5:N3	IN_800 (Input with clamps)	
	DDR-A6:N7	IN_800 (Input with clamps)	
	DDR-A7:P2	IN_800 (Input with clamps)	
	DDR-A8:P8	IN_800 (Input with clamps)	
	DDR-A9:P3	IN_800 (Input with clamps)	
	DDR-A10:M2	POWER	
	DDR-A11:P7	IN_800 (Input with clamps)	
	DDR-A12:R2	IN_800 (Input with clamps)	
	DDR_BA0:L2	GND	
	DDR_BA1:L3	DQ->DQ_FULL_800 (I/O with damps)	
	DDR_CAS#:L7	DQ->DQ_FULL_800 (I/O with damps)	
	DDR_CK0N:K8	DQ->DQ FULL 800 (I/O with damps)	
	DDR CK0P:J8	GND	
	DDR_CKE:K2	DO->DO FULL 800 (I/O with damps)	
	DDR CS#:L8	GND	
	DDR D0-R:G8	GND	
	DDR D1-R:G2	GND	
	DDR D2-R:H7	GND	
	DDR D3-R:H3	GND	
	DDR D4-R:H1	POWER	
	DDR D5-R:H9	POWER	
	DDR D6-R:F1	POWER	
	DDR D7-R:F9	POWER	
	DDR D8-R:C8	CLKIN 800 (Input with clamps)	
	DDR D9-R:C2	CLKIN 800 (Input with damps)	
	DDB_D10-B:D7	GND	
	DDB_D11_B;D2	CND	

ANSYS Automated Simulation Setup

Identify Component Pwr/Gnd Nets

Part Name	Ref. Des.	Supply 🔺	Power Net	Ground Net	Power Pin Group	Ground Pin Grou		
SQFP28X28_208	U1	Buffer Internal Voltage	VCC	GND	Group All	Group All		
SQFP20X20_144	U7	Buffer Internal Voltage	VCC	GND	Group All	Group All		
		Ground Net: (• Update	Ground Net Pin		•	Jpdate

ANSYS Automated Simulation Setup

Set Transient Simulation

SIwizard Step 4: Transient Simulation Options	
Options	
ANSYS Electronics Desktop Project Name	siwizard
Generate netlist instead of schematic	
Use ANSYS Electronics Desktop-Slwave Dynamic	
Include User-Defined Ports	
Transient Simulation Options	
Step Size	0.125s
Stop Time	125ns
Invoke Transient Simulation	
Plot Driver Waveforms	
Plot Receiver Waveforms	
Plot Power Rail Waveforms	
Invoke QuickEye Simulation	
S-parameter Options	
S-parameter Sweep Configuration	Edit
Signal Net Port Reference Impedance	50ohms
Power Net Port Reference Impedance	1ohms I I I I I I I I I I I I I I I I I I I
Force S-parameter Recomputation	
S-parameter Sweep Configuration	
	< Previous OK Cancel



Auto Generated AEDT Project and Transient Simulation Results



When Transient Analysis is complete, voltage/currents at the PCB terminals are "pushed" back to the field solver.



Power Integrity simulation - Basics

Fluid Dynamics

Structural Mechanics

Electromagnetics

Systems and Multiphysics

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DC Analysis

Fluid Dynamics

Structural Mechanics

Electromagnetics

Systems and Multiphysics

ANSYS Slwave - DC Analysis

• IR Drop

- Verify supplied voltage at all active parts

• Electromigration

- Verify maximum current denisity through vias
- Bottle Necks
 - Visualize regions of high current or voltage change

Perforated power and ground planes make for non-ideal DC supply rails Components with different proximity to VRM will have different supplied voltage Voltage seen at each load must remain within specified tolerances of chip



• DC Voltage Distributions



• Via and Bondwire Modeling



• DC Current Density Plots



Adaptive Mesh Refinement





- Place voltage source at VRM location
- Setup current sources at all IC loads; Pin by Pin or Total Current



DC Simulation Element Data							
Bondwires Current Sources	Vias	Voltage Probes	Vol	tage Sources			
		1					
Probe Name	Valu	e/V					
VPROBE_U0200_AA27_1	1.03	2994422649e+00	0				
VPROBE_U0200_Y28_1	1.03	3036287815e+00	0				
VPROBE_U0200_AB28_1	1.03	3378295162e+00	0				
VPROBE_U0200_AA29_1	1.03	3424868080e+00	0				
VPROBE_U0200_V20_1	1.03	4408546710e+00	0				
VPROBE_U0200_Y22_1	1.03	4414785251e+00	0				
VPROBE_U0200_Y24_1	1.03	4480893074e+00	0				
VPROBE_U0200_Y20_1	1.03	4496852552e+00	0				
VPROBE_U0200_AA23_1	1.03	4588522646e+00	0				
VPROBE_U0200_W19_1	1.034604139185e+000						
VPROBE_U0200_AA21_1	1.034612264663e+000						
VPROBE_U0200_V18_1	1.034627139438e+000						
VPROBE_U0200_AA25_1	1.03	4726999829e+00	0				
VPROBE_U0200_AB22_1	1.03	4773167804e+00	0				
VPROBE_U0200_Y18_1	1.03	4792394522e+00	0				
VPROBE_U0200_AA19_1	1.03	4815780404e+00	0				
VPROBE_U0200_AB24_1	1.034844478055e+000						
VPROBE_U0200_AB20_1	1.03	4856579405e+00	0				
VPROBE_U0200_AB18_1	1.03	5152306565e+00	0				
VPROBE_U0200_AA17_1	1.03	5207524112e+00	0				
VPROBE_U0200_Y16_1	1.03	5252125032e+00	0				
VPROBE_U0200_AB16_1	1.03	5587041452e+00	0				
VPROBE_U0200_AA15_1	1.03	5891159874e+00	0				
VPROBE_U0200_Y14_1	1.03	6026698599e+00	0				
VPROBE_U0200_Y30_1	1.03	6086352598e+00	0				
VPROBE_U0200_AB14_1	1.03	6338998195e+00	0				
VPROBE_U0200_AB30_1	1.03	6409611440e+00	0				
VPROBE_U0200_V22_1	1.03	6504100767e+00	D .				
VPROBE_U0200_AA31_1	1.03	6531319396e+00	U				
-							

Verify min/max voltages at all loads



٩	DC Simulation	Element Da	ata				
B	ondwires Current	t Sources Via	as 🛛 Voltage Probes 🗍 Voltage Sour	rces			
	Bondwire	Net	Current / A	Limit / A	Pass / Fail	Resistance (Obms	IR Drop / V
	Bondwire 0 Bondwire 1 Bondwire 2 Bondwire 3 Bondwire 4 Bondwire 5 Bondwire 6	NET-2 NET-2 NET-2 NET-2 NET-1 NET-1 NET-1 NET-1	3.323612005251e-001 3.287790889532e-001 3.388597269912e-001 -2.485415642892e-001 -2.515725644884e-001 -2.514511294508e-001 -2.484347582411e-001	±1.130973355292e+000 ±1.130973355292e+000 ±1.130973355292e+000 ±1.130973355292e+000 ±1.130973355292e+000 ±1.130973355292e+000 ±1.130973355292e+000	Pass Pass Pass Pass Pass Pass Pass Pass	2.018460548696e-001 2.035480772894e-001 1.981854524971e-001 2.221276000689e-001 2.193621761764e-001 2.193621761764e-001 2.221276000689e-001	6.708579711772e-002 6.692235140937e-002 6.715706832678e-002 -5.520794119293e-002 -5.518550521246e-002 -5.515886695836e-002 -5.515886695836e-002
			f Total current (I _{tot}) flowing through	↑ Current limit (I _{lim}) (see next		Electromigration "Pass" if I _{tot} <= I _{lin} "Fail" otherwise	check:
	Fit Selection		element	P-90)			

- Globally scan all vias and bondwires
- Reduce current density by adding additional vias to vicinity
ANSYS Bondwire/Via Current Limit

Define current limit (Ilim) as value above which electromigration is likely to be a problem

Computed using simple Ilim = tA formula

- t (A/m2): user-editable value in "dc_coeff.txt" (located in the Slwave V5 installation directory)
- A: cross-sectional area of conductor





Bondwire: $A = \pi r^2$ Via: $A = \pi (r_0^2 - r_i^2)$

1	# Ansoft Corporation
2	#
3	# SIwave DC Current Coefficients
4	# User-controllable values specified herein are used to set the
5	# maximum legal current magnitude in bondwires, solderballs,
6	<pre># solderbumps and vias</pre>
7	#
8	$\#$ Note: all values (except METAL_VOLTAGE and METAL_POWER) are in A/m^2
9	<pre># METAL_VOLTAGE is in volts</pre>
0	<pre># METAL_POWER is in W/m^2</pre>
.1	
.2	BONDWIRE 900e6
.3	SOLDERBALL 6e6
.4	SOLDERBUMP 60e6
.5	VIA 90e6
6	METAL_VOLTAGE 3.0
.7	METAL_CURRENT 5e6
8	METAL_POWER 5e4





Visualize where design improvements could be made



ANSYS Slwave - Zoom to problem Areas



Visualize Current on all layers to help determine a solution

INCLUDING The GND RETURN PATH

ANSYS Define Equipotential Regions for DC IR

- Equipotential regions are used by the DC IR drop solver to force equal voltage across a specified region, including specified pads.
- To define equipotential regions, click **Draw>Equipotential Regions**
- The cursor is activated to draw a rectangle. Use the menu selection to draw one or more regions on the Top or Bottom of the layout.
 - Hide all layers to see the regions



• Use the Delete All Regions button to erase any previously-defined regions

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Resonant Modes Analysis

Fluid Dynamics

Structural Mechanics

Electromagnetics

Systems and Multiphysics

ANSYS Resonance Simulation

Eigenmode analysis identifies location and frequency of natural cavity resonances that exist between planes

Scans entire PCB/PKG on all layers

If a resonance is excited, Signal Integrity can be compromised :

• High Z, null in S21, EMI etc.

Resonances should be moved away from critical parts and outside operating frequency

Reducing Resonance :

- Resonances always exist but you can reduce their impact by:
 - Changing the decoupling scheme
 - Changing the stackup
 - Changing plane dimensions
 - Adding via stitching
 - Moving discrete parts
- 186 © 2015 ANSYS, Inc. December 7, 2016

ANSYS Resonance Simulation : Rectangular Cavity

Structure: two metal planes, 60mm x 40mm

Dielectric: FR4 (er = 4.4, tan d = 0), 1 mm thick

Analytic solutions for voltage at resonance:

 $v(x, y) = \cos(n\pi x/a)\cos(m\pi y/b)$ n, m = 1, 2, 3, ...

Analytic solutions for resonance frequencies:

$$f_{nm} = \frac{c}{\lambda_{mn}} = \frac{c_0}{2\sqrt{\varepsilon_r}} \sqrt{\left(\frac{n}{a}\right)^2 + \left(\frac{m}{b}\right)^2}$$

m,n	Slwave (GHz)	Analytic (GHz)
1,0	1.192615376	1.19182823655
0,1	1.790103257	1.78774235483
1,1	2.154560548	2.14859890922
2,0	2.397284602	2.38365647311
2,1	3.000732847	2.97957059139

ANSYS Slwave Resonance Analyse

- Easy setup, no sources are required. To solve the resonant mode of the cavity using the Eigenmode solver :
 - Simulation > Compute Resonant Modes.
 - Enter the value for Minimum Frequency.
 - Enter the value for Maximum Frequency.
 - You can leave this field blank.
 - Specify the # of Modes to Compute.
 - The modes indicate the frequencies at which the cavity responds very strongly. This determines the voltage pattern between the top and bottom planes.

– OK

Resonant Mode Solution Options	
0.542GHz	ſ
Simulation name:	
Resonant Mode Sim 1 🔹	•
Find Modes in Frequency Range	
Minimum Frequency: 2.55238E+08 Hz	
Restore Recommended Minimum Frequency	
Maximum Frequency:	
# of Modes to Compute: 20	
Save Settings OK Cancel	

ANSYS Resonance Mode results

- Each mode is computed as well as several parameters.
- Re{f} corresponds to the frequency at which it will oscillate.
- Im{f} corresponds to the loss
- Wavelength(in vacuum) = c / Re{f}
- K = 2*pi / Wavelength
- Q = Re{f} / (2*pi*Im{f})

Display Voltage distribution between planes at resonance

- Red and blue areas indicate high impedances at a particular frequency
- Viewing Phase Animation
 - Select Metals plane
 - Compute
 - Generate Frames

	ant modes (nesona	ant Mode Sim 1)			
Mode	Be Fred (GHz)	Im Free (GHz)	k	Wavelength (m)	0
1	0.00010400	0.000077504	C 01 450000	0.000000005	Q 24 700521 000
1	0.329919403	0.006677094	6.31403333	0.308683323	24.708521600
2	0.673678026	0.011633947	14.11924737	0.440008010	28.957433200
3	0.535305373	0.010348071	14.09348149	0.430347386	33.010077700
4	0.744597133	0.010244096	19.50550195	0.402623707	35.344410200
		0.012300714	10.04027022	0.330002411	33.333742300
ſ	lot voltage dirrerence	e between planes on			Commute
l	L2	▼ and	L7	▼	
Mode	Plot Layer		Reference Layer		
1	L2		L7		
2	L2		L7		
3	L2		L7		
4	L2		L7		
5	L2		L7		
+1.000E	=+00¥	F	Phase Animation		Close
+1.000E +8.671E	=+00V =-01V	F	Phase Animation]	Close
+1.000E +8.571E +7.143E	=+00V =-01V =-01V	F	Phase Animation]	Close
+1.000E +8.571E +7.143E +6.714E	=+00¥ =-01¥ =-01¥	F	Phase Animation		Close
+1.000E +8.671E +7.143E +6.714E +4.286E	=+00V =- 01V =- 01V =- 01V	1	Phase Animation		Close
+1.000E +8.671E +7.143E +6.714E +4.286E +2.867E	=+00V =- 01V =- 01V =- 01V =- 01V	Į	Phase Animation		Close
+1.000E +8.571E +7.143E +5.714E +4.286E +2.857E +1.429E	=+00V =- 01V =- 01V =- 01V =- 01V =- 01V	F	Phase Animation		Close
+1.000E +8.571E +7.143E +5.714E +4.286E +2.867E +1.429E	=+00V =- 01V =- 01V =- 01V =- 01V =- 01V =- 01V		Phase Animation		Close
+1.000E +8.571E +7.143E +5.714E +4.286E +2.857E +1.429E	=+00V =- 01V =- 01V =- 01V =- 01V =- 01V =- 01V		Phase Animation		Close
+1.000E +8.571E +7.143E +5.714E +4.286E +2.857E +1.429E -1.429E	=+00V =- 01V =- 01V =- 01V =- 01V =- 01V =- 01V =- 01V		Phase Animation		Close
+1.000E +8.571E +7.143E +5.714E +4.286E +2.857E +1.429E -1.429E -1.429E	== 01V == 01V == 01V == 01V == 01V == 01V == 01V == 01V == 01V == 01V		Phase Animation		Close
+1.000 +8.571E +7.143E +5.714E +4.286E +1.429E -1.429E -1.429E -1.429E	5+00V 5-01V 5-01V 5-01V 5-01V 5-01V 5-01V 5-01V 5-01V 5-01V 5-01V 5-01V 5-01V 5-01V		Phase Animation		Close
+1.000E +8.671E +7.143E +5.714E +4.286E +2.067E +1.429E -1.429E -2.867E -4.286F	=+00V =- 01V =- 01V =- 01V =- 01V =- 01V =- 01V =- 01V =- 01V =- 01V		Phase Animation		Close
+1.000E +8.671E +7.143E +6.714E +4.286E +4.286E +1.429E -1.429E -1.429E -4.286E -5.714E	5+00V 5-01V 5-01V 5-01V 5-01V 5-01V 5-01V 5-01V 5-01V 5-01V 5-01V 5-01V 5-01V 5-01V 5-01V 5-01V		Phase Animation		Close
+1.000E +8.671E +7.143E +4.286E +4.286E +1.429E -1.429E -2.867E -2.867E -4.286E -5.714E -7.143E	=-00V =-01V =-01V =-01V =-01V =-01V =-01V =-01V =-01V =-01V =-01V		Phase Animation		Close

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Frequency Sweep Analysis

Fluid Dynamics

Structural Mechanics

Electromagnetics

Systems and Multiphysics

ANSYS Frequency Sweep Analysis Review

- Although resonant modes are inevitable, they may or may not be excited depending on the location of the source.
- With the Frequency Sweep Analysis, the designer can excite the design in specified locations and see the aggregate response of all the resonant modes of the board for the given source location.
 - Verify maximum IR drop across frequencies



Frequency Sweep

- Current or voltage sources
- Voltage distribution at all desired frequencies.
- Voltage probes for quantitative dependence.



+1.157E-04V

ANSYS Why Resonances Mode Analysis?

- Return path current is disrupted at the via.
- Signal vias couple to the planes.
- Creates a feed for the parallel plate waveguide.



ANSYS Simple Slwave Experiment

Control Case :

 Microstrip transmission line without a via transition

Test Case :

Same length transmission line with a via transition from top to bottom

4 Layer 8x10" PCB





Control Case



Test Case



• The blue and the red represent the resonance points. Where green has no

resonance.

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ANSYS Far Fields at 3 Meters





Computing Impedance of PDN using S-,Y-, Z- Analysis

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ANSYS Plane impedance Simulation

- Same setup as S-Parameter extraction. Place ports in locations of interest. Pin Grouping can be useful
- Verify low impedance up to device cut-off frequency



ANSYS Slwave : Grouping Pins

You can create pin groups for various components. The grouped pins will be treated as if they were electrically connected during the analysis.

You can use this pin group to create ports

- Tools > Create/Manage Pin Groups...
- Double click on the IC component in the 3D modeler



Create/Manage Pin Groups		• •	X
Part Name: SQFP28X28_208	•	Options Create pin groups for each	part
Reference Designator: U1 U2		 Create pin groups for each Create pin groups per grid Row # 3 Col # Delete existing pin groups 	net cell : 3
Nets List common nets only Display Pin Name FIBON4 FIBOP3 GND GNDB HOLDCOL IR 10CFS IR 10CLK IR 10COL IR 10DAT IR 10DEN IR 100CN IR 100CLK IR 100CLK IR 100CLK IR 100CLK IR 100CL	 Net Selection Select all nets Unselect all nets Net Visibility Show All Nets Hide All Nets 	Pin Group List U2_GRP_0_0_GND U2_GRP_0_1_GND U2_GRP_0_2_GND U2_GRP_1_2_GND U2_GRP_1_2_GND U2_GRP_2_0_GND U2_GRP_2_2_GND Create Pin Group(s) Delete Pin Group(s) Edit Pin Group	Naming Convention Create Port Create Terminal



ANSYS Pin grouping port between different components

Create a Pin Group from multiple components:

Multi-select Pins in GUI

• RT click -> Create/Manage Pin Groups...

December 7, 2016



ANSYS S-,Y-, Z- Analysis

- To extract S, Y and Z matrix for the predefined ports :
 - Simulation > Compute S-,Y-,Z-parameters
 - Enter the value for Start Frequency.
 - Set the stop frequency or rise time information
 - (Frequency Bandwith= 0.5/min rise time)
 - Specify the Number of Solution Points.
 - Select the method for distributing points
 - Choose the sweep Selection
 - Discrete sweep
 - Interpolating sweep

Comput	e S	YZ-parameter	rs	10.00		X			
Sweep	Sweep Sensitivity Distributed Analysis (HPC)								
Si	Simulation name: SYZ Sweep 1 -								
	Compute exact DC point								
Fr	Frequency Range Setup								
		Start Freq	Stop Freq	Num. Points / Step Size	Distribution				
	1	1Hz	1GHz	20	By Decade				
	2	1GHz	5GHz	100	Linear				
		Add Above	Add Below	Delete Selection	Preview				
Sw	vee D	p Selection iscrete Sweep		Set FWS genera	ation paramet	ers			
				Min Rise/Fall T	īme / s				
				1E-10					
	Contempolating Sweep Relative error for 5: 0.005								
				Other solver opti	ons				
		ert Touchatana	© fla aftar sim	ulation completes					
	xp		w nie arter sin	iulauon completes					
F	File	path: E:\SVN	_Training\SIwa	ave\input_files\WS01_2\s	iwaveB	rowse			
				Save Settings	Launch	Close			

ANSYS Frequency Sweep Selection box

Discrete Sweep:

• All frequency points in the list are solved. Look at the Frequency List Preview.

Interpolating Sweep:

• Following an Error tolerance, an interpolating sweep estimates a frequency response for an entire frequency range by solving at a relatively small number of frequency points within that range. Between the actual solution frequencies, the frequency response is obtained by rational interpolation. Slwave adaptively chooses the frequency points at which it computes the field solution. After a new frequency point is solved, a new interpolating fit is generated. This is compared to the interpolant from the previous step, and the maximum difference between the two is determined. If the difference exceeds the requested tolerance, then a new frequency point is chosen for a solution. The interpolating sweep is complete when the difference between successive interpolants is less than the error tolerance criterion.

Optionally, to save these settings and use them for subsequent simulations, click the Save Settings button

Frequency List Preview



• During simulation, in the Process Monitor workspace, you can follow the simulation progress. profile, monitoring the real time, CPU time, memory requirements and view the matrix informations.

Process Monitor (SYZ Sweep 1)	
Display: Messages 🔹 🖬 🕨	
Solving for DC voltage/current distribution Initializing the problem Setting up solution materials Reading geometry file Reading layer stack up	^
Setting up circuit graph Creating 6 layer meshes Meshing Layer #1 Meshing Layer #2 Meshing Layer #3 Meshing Layer #6	E
4	Þ
Setup: 100%	
Simulation: 35%	
Messages Process Monitor (SYZ Sweep 1)	

- When the simulation is done, the profile is available with real time, CPU time, memory requirements and view the matrix informations.
- Results > Analysis Name > View profile

	Real Time	CPU Time	Memory	512 e	
commenced o	wave_ng 5.0.0 on host LYOR	D (Built: No FERNAND7L at	V 4 2010 (Mon Feb 0)	04:34:46) 7 22:18:26 2011	
Command	Real	Cpu Time	Memory		-
geomproc solve_setup	00:00:02	00:00:01	12276K 57780K	2040 triangle 1 project	
Finished on LYOR	RFERNAND7L at	t 02/07/2011	22:18:30		-
SIW	ave 5.0.0 No	9 2010 at	11:47:27	beginning	
I	Real	Cpu	Memory		
Command	Time	Time	111284	Number of Elements	
xsec_solve	00:00:00	00:00:00	23524K	7 xsections	
via_extract	00:00:00	00:00:00	23524K	10346 triangles	
DRS 20	00:00:04	00:00:00	73280K	21162 matrix	
SIWave	00:00:02	00:00:01	73280K	21162 matrix	i
Finished on LYOR	RFERNAND7L at	t 02/07/2011	22:18:37		-
AC Solution Prof	file:			ci	
	Real lime	CPO TIme	Memory	5126	
Module					

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Sensitivity Analysis

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Structural Mechanics

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ANSYS Sensitivity Analysis

Sensitivity analysis computes the derivative of a circuit response (an S-, Y- or Z-parameter) with respect to the impedance of a circuit element, typically a decoupling capacitor.

Therefore it is a measure of how much that output parameter will change in response to a change in the circuit element.

- A low sensitivity indicates that the circuit element has little influence on the circuit response of interest
- A high sensitivity indicates that the response is a strong function of the circuit element.

This information can help a designer to identify which circuit elements need to be adjusted to improve a circuit response. It can be used to find unnecessary decoupling capacitorsones that aren't affecting the results significantly. It can also help to identify which circuit elements need loose or tight tolerances.

ANSYS Sensitivity Analysis

- Advantages :
- Sensitivity analysis can be computed very quickly for a large number of circuit elements once you have solved for the nominal S-parameters.
- Using the built-in sensitivity analysis capability, you can reduce that time to a small fraction (perhaps 5%) of the analysis time for the nominal problem. It is essentially "free" information

ANSYS Sensitivity Analysis in details

The software internally computes the derivative the circuit responses that you designate with respect to the impedance of the circuit elements you choose. To make this more concrete, suppose you pick an Sparameter *Sij* and a capacitor *C*. The impedance of the capacitor is *Zc=jwC*. So the software computes the derivative, *dSij/dZc*.

This "raw" derivative is then normalized as follows to make it easier to interpret:

normalized sensitivity =
$$\frac{dS_{ij}}{dZ_c} \cdot \frac{Z_c}{S_{ij}} = \left(\frac{dS_{ij}}{S_{ij}}\right) / \left(\frac{dZ_c}{Z_c}\right)$$

- As shown in the formula above, the normalized sensitivity can be interpreted as the ratio of the fractional change in the output parameter to the fractional change in the impedance of the circuit element. So if the normalized sensitivity is 10, that would indicate that a 1% change in the capacitor's impedance would result in a 10% change in the output S-parameter. Normalized sensitivity makes it easy to compare the sensitivities of circuit elements with widely varying impedances.
- The normalized sensitivity is a complex number. The software reports the magnitude of the normalized sensitivity, so what you see in the user interface is a real number.

ANSYS Capacitors Name Visibility

Change visibility settings for element names :

• Visibility > Labels > Capacitors

Adjust the size of the text

• Visibility > Labels > Change Text Attributes...

			<i>265</i>		CLB CLB C C C C C C C C C C C C C C C C	¢67
Resistors Ports	Pins	Ĵ≣ Circuit Element Values ▼		Ø	Value: 1E-0/F + Net: VCC - Net: GND	
Inductors Probes / Sources	Bondwires	📑 Change Text Attributes	C27	● C71		
Capacitors 🗌 IC / IO / Discrete De	evices Solderballs					
	Labels					
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ANSYS°

Set sensitivity computation for capacitors, inductors and inductors

Edit > Circuit Element Parameters.

• Select capacitors that will be available for sensitivity analysis

RLC_XYZ_C C69 RLC_XYZ_C C68 RLC_XYZ_C C67 RLC_XYZ_C C66 RLC_XYZ_C C65 CAPACITO C39	1E-07 1E-07 1E-07 1E-07	1E-11 1E-11 1E-11	0 0	VCC VCC	GND E
RLC_XYZ_C C68 RLC_XYZ_C C67 RLC_XYZ_C C66 RLC_XYZ_C C65 CAPACITO C39	1E-07 1E-07 1E-07 1E-07	1E-11 1E-11	0	VCC	GND =
RLC_XYZ_C C67 RLC_XYZ_C C66 RLC_XYZ_C C65 CAPACITO C39	1E-07 1E-07	1E-11	0		
RLC_XYZ_C C66 RLC_XYZ_C C65 CAPACITO C39	1E-07	15 11	U U	VCC	GND
RLC_XYZ_C C65 CAPACITO C39	1E 07	1E-11	0	VCC	GND
CAPACITO C39	1E-07	1E-11	0	VCC	GND
	1E-07	0	0	GND	VCC
RLC_XYZ_C C/3	1E-07	1E-11	0	VCC	GND
RLC_XYZ_C C74	1E-07	1E-11	0	VCC	GND
RLC_XYZ_C C72	1E-07	1E-11	0	VCC	GND
CAPACITO C27	1E-07	0	0	GND	VCC
CAPACITO C28	1E-07	0	0	GND	Compute SY7-parameters
CAPACITO C38	1E-07	0	0	GND	
RLC_XYZ_C C71	1E-07	1E-11	0	VCC	Sweep Sensitivity
RLC_XYZ_C C70	1E-07	1E-11	0	VCC	
CAPACITO C18	1E-07	0	0	GND	Matrix Entry S Y Z
CAPACITO C10	1E-07	0	0	GND	
CAPACITO C9	1E-07	0	0	GND	
CAPACITO C12	1E-07	0	0	GND	
	45.07		Ĵ	0110	
Modify Layers	Delete	Fit Selection	Activ	/ate	
	RLC_XYZ_C C72 CAPACITO C27 CAPACITO C28 CAPACITO C38 RLC_XYZ_C C71 RLC_XYZ_C C70 CAPACITO C18 CAPACITO C10 CAPACITO C9 CAPACITO C12 III	RLC_XYZ_C C72 1E-07 CAPACITO C27 1E-07 CAPACITO C28 1E-07 CAPACITO C38 1E-07 RLC_XYZ_C C71 1E-07 RLC_XYZ_C C70 1E-07 CAPACITO C18 1E-07 CAPACITO C10 1E-07 CAPACITO C12 1E-07 CAPACITO C12 1E-07 III	RLC_XYZ_C C72 1E-07 1E-11 CAPACITO C27 1E-07 0 CAPACITO C28 1E-07 0 CAPACITO C38 1E-07 0 RLC_XYZ_C C71 1E-07 1E-11 RLC_XYZ_C C70 1E-07 1E-11 RLC_XYZ_C C70 1E-07 0 CAPACITO C18 1E-07 0 CAPACITO C10 1E-07 0 CAPACITO C12 1E-07 0 CAPACITO C12 1E-07 III	RLC_XYZ_C C72 1E-07 1E-11 0 CAPACITO C27 1E-07 0 0 CAPACITO C28 1E-07 0 0 CAPACITO C28 1E-07 0 0 CAPACITO C38 1E-07 0 0 RLC_XYZ_C C71 1E-07 1E-11 0 RLC_XYZ_C C70 1E-07 1E-11 0 CAPACITO C18 1E-07 0 0 CAPACITO C10 1E-07 0 0 CAPACITO C12 1E-07 0 0 <td>RLC_XYZ_C C72 1E-07 1E-11 0 VCC CAPACITO C27 1E-07 0 0 GND CAPACITO C28 1E-07 0 0 GND CAPACITO C28 1E-07 0 0 GND CAPACITO C38 1E-07 0 0 GND RLC_XYZ_C C71 1E-07 1E-11 0 VCC RLC_XYZ_C C70 1E-07 1E-11 0 VCC CAPACITO C18 1E-07 0 0 GND CAPACITO C10 1E-07 0 0 GND CAPACITO C10 1E-07 0 0 GND CAPACITO C12 1E-07</td>	RLC_XYZ_C C72 1E-07 1E-11 0 VCC CAPACITO C27 1E-07 0 0 GND CAPACITO C28 1E-07 0 0 GND CAPACITO C28 1E-07 0 0 GND CAPACITO C38 1E-07 0 0 GND RLC_XYZ_C C71 1E-07 1E-11 0 VCC RLC_XYZ_C C70 1E-07 1E-11 0 VCC CAPACITO C18 1E-07 0 0 GND CAPACITO C10 1E-07 0 0 GND CAPACITO C10 1E-07 0 0 GND CAPACITO C12 1E-07

Save Settings

OK

Cancel

Help

ANSYS Results >SYZ > Plot Sensitivity

Here, the max normalized sensitivity is 26.8 for C71 :

• It indicate that a 1% change in the capacitor's impedance would result in a 26.8% change in the output Z-parameter.



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Power Distribution System & PI Methodology

Fluid Dynamics

Structural Mechanics

Electromagnetics

Systems and Multiphysics

ANSYS Power Distribution System

PDS Design Goal:

- Reduce noise in the power distribution system to a level that is acceptable for system performance.
- System Engineer $\Delta V(\omega)$ Acceptable Ripple Voltage
- Active Device Current Spectrum

 $\Delta I(\omega)$ Current Spectrum

Power Distribution Impedance Specification

 $Z(\omega) =$

Target Impedance

ANSYS Target Impedance of PDS



- 1. The Impedance looks into PDS at the device should be kept low over a broad frequency range (from DC to package cut-off frequency)!
- 2. The Desired Frequency Range and Impedance Value is called Target Impedance.
- Target impedance goal is set with the help of allowable ripple on the power/ground plane over a specified frequency range.
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ANSYS Target Impedance Calculation & Trends

$$Z_{\text{Target}} = \frac{(Power _Supply _Voltage) \times (Allowed _Ripple)}{Current}$$
$$Z_{\text{Target}(2.5v)} = \frac{(2.5V) \times (5\%)}{40.3A} = 3.1m\Omega$$

Target Impendence is the goal that designers should hit!

Year of first production	1997	1999	2002	2005	2008
Chip technology	0.25um	0.18um	0.13um	0.10um	0.07um
Across Chip Frequency (MHz)	450	600	800	1000	1100
Max. Chip Power (W)	100	120	140	160	180
Max current (A)	40.3	66.7	93.3	133.3	180.0
Power Supply (V)	2.5	1.8	1.5	1.2	0.9
Target Impedance $(m\Omega)$	3.1	1.3	0.8	0.45	0.25

*Source: International Technology Roadmap for Semiconductors

December 7, 2016

^{*}Target Impedance is falling ~ 1.6x, every 3 years



Impedance consists of

- Capacitive factor, decreases with frequency
- Inductive factor, increases with frequency
- Inductance includes plane inductance, ESL of decoupling capacitors, traces and vias which connect planes to capacitors

 $2\pi f L$

1

 $2\pi f C$



ANSYS Core Power Delivery Network


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Merging Package on Board

Fluid Dynamics

Structural Mechanics

Electromagnetics

Systems and Multiphysics

ANSYS Connect a package onto a PCB

- Tools > Attach Package Design...
- Some recommendations :
 - The project of the board must be opened
 - Identify the package location.
 - Identify the Part Name, Designator Name of the Package.
 - Identify a specific net in the board and package side to know if a rotation is needed.
- Attach Package Design...

• Package Padstack



ANSYS Connect a package onto a PCB

- Enter the Package Path
- Select the solderballs model and parameters
- Select the PCB Part Name and PCB Reference Designator
- Align pins using pins selection
 - Automatic
- Select Merging options
 - Merge Layers
 - Merge nets
 - Generate solderballs
- Execute Merge

📧 Attach Package	_	×
Package Package Path: J:\Package.siw Solderball Parameters Height: 22.000000 mils Radius: 11.000000 mils Add solderballs to following package padstack: 0201	Browse	Package Rotation Angle Enter an angle in degrees. Otherwise select two pairs of pins from package and PCB to be mapped. (yellow to yellow, red to red) Rotation Angle: 0 degrees Pan: Hold left mouse button and drag Zoom: Mouse wheel Selection: Click left mouse button
Package View		All Alt Selected PCB Pins Alt Alt Merge Options Merge Lavers
PCB Placement Layer: TOP PCB Part Name: SMD_VT3275_BGA865 Ilist All Parts	Fit All	Generate Solderballs Generate Solderballs Merge Nets Net Merge Options O Preserve Package Net Names O Preserve PCB Net Names Export Connection Info
PCB Reference U16		3:/PCB.connectionInfo Change File Name
Number of selected designators: 1 PCB View © View Selected Only © View All	Fit All	Execute Merge Cancel



WS06_0_siwave_pkg_pcb_merge.pdf



Chip-Package-PCB Co-Design using S-Parameters

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ANSYS ANSYS Chip-Aware PDN Solution

- Redhawk generates a chip power model (CPM) including chip PDN parasitics and switching currents.
- Slwave provide robust extraction of IC packages and boards with broadband S-parameter models.
- PI Advisor optimizes decoupling capacitor selection to meet a target impedance.
- AEDT simulates power noise in the time domain.



ANSYS What's in a CPM?

PCB + Package



SUBCKT PowerModel p1 p2

Each C4 bump (power & ground) will be associated to its corresponding:

✓ Chip PDN RLC

Physical model of chip layout

✓ Transistor/cell current /cap/ESR
Electrical model of chip layout

CPM is topological, physical and activity based

* Apache RedHawk Chip Power Model [Accurate RC reduction] ********* Apache RedHawk Chip Power Model [Ver 1.00] Version: 10.2 Linux32e3 (Jan 20 00:31:13 2011) * Pad name DPOWER21 INCLUDE "PowerModel.sp.inc" DGROUND20 * Begin Chip Package Protocol ---> * No connec * die_area 0 0 4920.62 5000.36 CO 1 p1 p2 * Start Units Length um R_1_1 p1 n3 * End Units C_1_1 n3 p2 (4905.000000 3279.000000) (4880.000000 3219.000000) = PAR 0 0 VDD * DPOWER21 p1 R_2_1 p1 n4 p2 * DGROUND20 = PAR 0 0 VSS C_2_1 n4 p2 R_3_1 p1 n5 * End Chip Package Protocol <---</p> C_3_1 n5 p2 .subckt adsPowerModel p1 p2 R_4_1 p1 n6 C_4_1 n6 p2 Xpdn p1 p2 PowerModel ENDS Icursig1 p1 p2 pw1(+ 0.000000ps 0.589435 + 150.000000ps 0.854897 + 240.000000ps 0.867186 + 330.00000ps 0.827372 223 December 7, 2016 D 2015 ANSYS, Inc.





ANSYS Slwave CPM Integration

- Slwave CPM integration includes the following:
- Import of die PDN for inclusion in frequencydomain extractions
- Automatic matching of die pin to CPM pin locations



ANSYS Slwave CPM Setup

- Select the device footprint in the SIwave layout
- File > Import > Apache CPM/PLOC file...
 - Browse to the CPM file
- Click the **Auto Connect** button to attach Slwave footprint pins to the CPM pins.

Apache CPM/PLOC Import	Apache CPM/PLOC Import
Part Name: FCHIP Reference Designator: FCHIP	Part Name: FOHIP Reference Designator: FOHIP
IC Die Information	IC Die Information
CPM File: E:\Ansoft Project\Siwave_Projects\SIwave - CPM file_PDN ChipPackagePCB\Package_ Browse	CPM File: E:\Package_Demo\cpm.sp Browse Pins mapped: 106 Pins unmapped: 0
Rotation in degrees (counter dockwise): 0 Update	Rotation in degrees (counter dockwise): 0 Update
Location of die center on package: (0.000000, 0.000000) Update	Location of die center on package: (0.000000, 0.000000) Update
Flp Die Reset Auto Connec Manual Connect Create Pin Groups Export Connection Information	Flip Die Reset Auto Connect Manual Connect Create Pin Groups Export Connection Information
Package Pins	Package Pins
Index Pin Name X Y Net Connected Die Pin Die Pin Index	Index Pin Name X Y Net Connected Die Pin Die Pin Index
1 A1 -1.91 1.91 FCHIP_A1 2 A2 -1.69 1.91 FCHIP_A2 3 A3 -1.46 1.91 FCHIP_A3 4 A6 -0.79 1.91 FCHIP_A6 5 A7 -0.56 1.91 FCHIP_A7 6 A9 -0.11 1.91 VDD_15 8 A12 0.56 1.91 FCHIP_A13 9 A13 0.79 1.91 FCHIP_A13 Add One Pair Delete ALL Pairs Delete One Pair Delete ALL Pairs	1 A1 -1.91 1.91 FOHP_A1 2 A2 -1.69 1.91 FOHP_A2 3 A3 -1.46 1.91 FOHP_A3 4 A6 -0.79 1.91 FOHP_A7 5 A7 -0.56 1.91 FOHP_A7 6 A9 -0.11 1.91 VDD_15 bumpnode_151#a10 2 7 A10 0.11 1.91 VDD_15 bumpnode_151#a10 2 4 8 A12 0.56 1.91 FOHP_A13 - - - Add One Pair Delete One Pair Delete ALL Pairs Pin Pair Connect
Index Pin Name SPICE Node Group Name Group Net Ref. Group Name Package Pin	Index Pin Name SPICE Node Group Name Group Net Ref. Group Name Package Pin
1 bumpnode_150#a9 p3 VDD_15_FCHIP_VDD_15_2	1 bumpnode_150#a9 p3 VDD_15_FCHIP_VDD_15_2 VDD_15 VSS_FCHIP_VSS_2 A9
2 bumpnode_151#a10 p3 VDD_15_FCHIP_VDD_15_2	2 bumpnode_151#a10 p3 VDD_15_FCHIP_VDD_15_2 VDD_15 VSS_FCHIP_VSS_2 A10
3 bumprode_158#b2 p4 VSS_FCHP_VSS_2 4 bumprode_158#b2 p3 VDD_16_2	3 bumpnode_158#b2 p4 VSS_FCHIP_VSS_2 VSS B2
5 bumprode 164#98 p3 VDD 15 FCHP VDD 15 2	tumpnote_165#b0/ p3
6 bumpnode_165#b9 p3 VDD_15_FCHIP_VDD_15_2	6 bumpnode_165#b9 p3 VDD_15_FCHIP_VDD_15_2 VDD_15 VS5_FCHIP_VS5_2 B9
7 bumpnode_166#b10 p3 VDD_15_FCHIP_VDD_15_2	7 bumpnode_166#b10 p3 VDD_15_FCHIP_VDD_15_2 VDD_15 VSS_FCHIP_VSS_2 B10
8 bumpnde_167#b11 p3 VDD_15_FCHIP_VDD_15_2	8 bumpnode_167#b11 p3 VDD_15_FCHIP_VDD_15_2 VDD_15 VSS_FCHIP_VSS_2 B11
Operations Marco solution groups on some opt	Operations
Change reference group for to VDD_15_FCHIP_VDD_15_2 V Update OK Cancel	Merge selected groups Merge groups on same net Change reference group for to VDD_15_FCHIP_VDD_15_2 Update OK Cancel



- CPM Impedance Effect
- There is a significant effect at a broad frequency range due to the high total capacitance present on this chip.



ANSYS AEDT, Slwave, and CPM







ANSYS Simulation approaches

- The PI methodology is different depending on the needs. We can considered two simulation approaches.
 - « Free optimization » of a design (The location, mounting style, value, number and type of capacitors are not predefined).
 - « Fixed » optimization of an existing design. The location of capacitors are already fixed (footprint defined as discrete device during database import). The max number of capacitor is also predefined.
 - PI Optimization using SIwave and ANSYS AEDT (Iterative Approach)
 - PI Optimization using Pladvisor (An Automated Approach)

ANSYS Free optimization of a design

- Place Probe on different power nets to scan all the frequency range. EM extraction of impedance for critical devices :
 - SYZ analysis
 - Compare to the defined target
- Resonances analysis is performed to evaluate problems on power planes and helping the placement of decoupling capacitors :
 - Resonance and frequency sweep analysis
 - Choose some decoupling capacitors to move the resonances in terms of Impedance magnitude and Resonance frequency
 - Capacitor Library Browser
 - Place them close to the resonance peaks
- The final step is to simulate in time domain to check for compliance. Look at the Switching Power Noise
 - Transient simulation in AEDT

ANSYS The Capacitor Library Browser

- Explore and plot the impedance of various vendor or imported capacitor components versus frequency and quickly determine the lumped circuit equivalent (Included with Slwave)
 - Capacitor Library Browser # ㅈ ㅋ ㅋ ㅋ ㅋ ㅋ ㅋ Impedance 1E3 1E2 1E1 |Z11| [ohm] 1E0 1E-1 1E-2 1E-3 1E-2 1E-1 1E0 1E1 1E2 1E3 1E4 Frequency [MHz] ESR (ohms) Vendor Series Part Name Plot Value (F) # Ac EIA Size Price L_mnt (H) R_mnt (ohms) SRF (Hz) S_min (dB) ESL (H) AVX 0306 0306ZC103KA 1 1E-08 3 0306 0.01 1E-09 0.001 9.03649E+07 -60.2637 0.0973991 3.10199E-10 AVX NOJ 3.3E-06 Other 1E-10 0.001 9.8506E+06 0.7041 7.91045E-11 NOJP335K010R 2 0 -43 2659 Murata GRM55 GRM55RF51H475ZD01 V 4.7E-06 2 2220 0.01 1E-09 0.001 3.23661E+06 -80.5035 0.00940348 5.14471E-10 AVX 0201 02013A180JA V 1.8E-11 0201 0.01 1E-09 0.001 2.18148E+09 -52.7179 0.181549 2.95709E-10 TDK C3216-MidVoltage C3216C0G2J121J(K) 1 2E-10 1206 0.01 1E-09 0.001 4.50331E+08 -58 4244 0 119116 1 04087E-09 GCM155R71H102KA37 1E-09 0402 0.01 1E-09 0.001 -50.9926 0.280801 4.02783E-10 Murata GCM15 2.50775E+08 YUDEN Standard Class1 1005(0. UMK105CH331 3.3E-10 1 0402 0.01 1E-09 0.001 4.00222E+08 -53.1304 0.220793 4.79208E-10 Kemet T493A T493A104M035AH6X10 1E-07 1206 0.01 1E-09 0.001 4.99649E+07 -35.2078 1.80002 1.01464E-10 👻 Use selected capacitor model for part CAPACITOR CDR02 Apply Price -Update Filters Vendor Show Series Show . EIA Size Show . Min. Max. Filter Quantity 1 1 AVX \checkmark 0201 01005 Value (F) 1E-13 0.0015 Ε 1 0306 1 0201 V SRF Range (Hz) 0 2.10375E+10 Kemet Murata \checkmark 0402 1 0306 1 S_min Range (dB) -106.911 -7.97224 **V v** Panasonic 7 0508 0402 ESR Range (ohms) 4.99788E-05 593486 \checkmark Samsung 0603 0508 ESL Range (H) 0 0.451721 -7 **V** TDK 0612 0603 Price 0.01 0 7 7 7 0805 0612 YUDEN 7 7 1206 0805 Load Filters. Save Filters...
 - Tools > Capacitor Library Browser

ANSYS PI Optimization using Slwave and ANSYS AEDT (Iterative Approach)

- A very useful technique for evaluating the effectiveness of the capacitors and there locations is to extract the model into AEDT.
 - In Slwave, place a port at the IC and replace the capacitors you are interested in optimizing with a port.
 - After, run a SYZ simulation and import the s-parameters into AEDT.
 - Place a port again at the IC terminal and connect the capacitors from the other terminals to ground.
 - Now, when you run a linear network analysis, you can see the same results as in Slwave but it will be much quicker.
 - This allows you to try many different combinations of capacitors and optimize them.



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SimplePI using Capacitor Library Browser

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ANSYS The Capacitor Library Browser (1/2)

Explore and plot the impedance of various vendor or imported capacitor components versus frequency and quickly determine the lumped circuit equivalent (Included with SIwave)

• Tools > Capacitor Library Browser



ANSYS The Capacitor Library Browser (2/2)

- Automatically determine the best type and number of capacitors given a frequency dependent impedance mask and mount capacitors at certain userdefined capacitor regions.
 - (Pladvisor is mandatory)
- Define VRM parameters, Load an impedance Mask and then Run « Auto select capacitors required to match impedance profile »





• Two Statistics are provided, Siwave optimize the numbers of capacitors used and the types.



MOUNT THE PROVIDED SOLUTION IN THE EXISTING DESIGN

Capacitor Library Browser

H Mount active capacitors in design

- Select « Mount active Capacitors in design »
- 4 steps are required to mount a capacitor.

Capacitor Mounting Dialog					
Options	- Unmounted C	apacitors			
Mounting Style: 2 Via Wide 🔻	Vendor	Series	Part Name	Value	Size
1	Murata	GRM03	GRM033R71E121KA01	1.2E-10	0201
	Murata	GRM03	GRM033R71C331KD01	3.3E-10	0201
	Murata	GRM03	GRM033F51A222ZD01	2.2E-09	0201
	Murata	GRM15	GRM1555C1H161JA01	1.6E-10	0402
	Murata	GCM21	GCM21BR71H104KA37	1E-07	0805
	Murata	GRM31	GRM3195C1H133JA01	1.3E-08	1206
	Murata	GRM32	GRM32ER61E226KE15	2.2E-05	1210
	Mounted Cap	acitors	Part Name	Value	Size
		Junes		YUICE	JEC
Edit Mount Dimensions					
Connect between nets					
P28VA	_		Unmount Selection		
GND -					Close

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Mount the provided solution in the existing design (3/4 steps)

- For each unmounted capacitors, SIwave allow you to choose :
- The Mounting style (2 via Tall or 2 via Wide)
- Define the Capacitors Mount Dimensions
- Define the connected nets

Capacitor Mount Dimensions				a summer	184		×
	514.0	5		D 10	▼ 146 14 7 4 5	- 1 - 4 / 43	
	EIA Size	Pad Width (mils)	Pad Height (mils)	Pad Spacing (mils)	Trace Width (mils)	Trace Length (mils)	Via Padstack
	01005	30	20	10	5	20	Auto Generate
	0201	30	20	10	5	20	Auto Generate
	0306	30	20	10	5	20	Auto Generate
	0402	30	20	10	5	20	Auto Generate
	0508	30	20	10	5	20	Auto Generate
	0603	30	20	10	5	20	Auto Generate
└ ── ── <u>₩</u> -₩-₩-	0612	30	20	10	5	20	Auto Generate
	0805	30	20	10	5	20	Auto Generate
	1206	30	20	10	5	20	Auto Generate
	1210	30	20	10	5	20	Auto Generate
	1310	30	20	10	5	20	Auto Generate
	1632	30	20	10	5	20	Auto Generate
\longleftrightarrow	1808	30	20	10	5	20	Auto Generate
W	1812	30	20	10	5	20	Auto Generate
U. Dad Usiaht	1825	30	20	10	5	20	Auto Generate
H: Pad Height	2220	30	20	10	5	20	Auto Generate
W: Pad Width	2225	30	20	10	5	20	Auto Generate
S: Pad Spacing	2312	30	20	10	5	20	Auto Generate
TL: Trace Length	2816	30	20	10	5	20	Auto Generate
TW: Trace Width	2823	30	20	10	5	20	Auto Generate
	Import	Export				ОК	Cancel
							-



Connect between nets	3		
P28VA		•	and
GND		•	

ANSYS[®]

Mount the provided solution in the existing design (4/4 steps)

The last step to allow the mounting is to define a capacitor region on the layout

- Draw > Capacitor regions...
 - Select the top or bottom region
- Use the mouse to draw a rectangle

0 ie : 2 regions θ 6 0 Ö o 0 00000 241 © 2015 ANSYS, Inc. December 7,

Define Capacito	efine Capacitor Regions							
Flavo K ar								
Elevation	n of Region							
Te	op							
🔘 B	ottom							
Delete A	All Regions							
(Close							

ANSYS Mount the provided solution in the existing design (Final step)

Select the pre-defined regions and Unmounted Capacitors and click « Mount Selection »

Capacitor Mounting Dialog		The state	1 m				
Options	Unmounted	Capacitors					
Mounting Style: 2 Via Wide	Vendor	Series	Part Name	Value	Size		
	Murata	GRM03	GRM033R71E121KA01	1.2E-10	0201		
	Murata	GRM03	GRM033R71C331KD01	3.3E-10	0201		
	Murata	GRM03	GRM033F51A222ZD01	2.2E-09	0201		
	Murata	GRM15	GRM1555C1H161JA01	1.6E-10	0402		
	Murata	GCM21	GCM21BR71H104KA37	1E-07	0805		
	Murata	GRM31	GRM3195C1H133JA01	1.3E-08	1206	\	
	Murata	GRM32	GRM32ER61E226KE15	2.2E-05	1210		
	•				- F	/	
			Mount Selection			V	
Edit Mount Dimensions Edit Mount Dimensions Connect between nets P28VA • and GND •	Mounted Caj	Series	Part Name Value	Size	Close		Capacitor (Active) Name: C89 Value: 2.2E.09F + Net: P28VA - Net: GND

• Note : If some capacitors can not be mount due to their size / area constraints, the following message appears.



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ANSYS Power Integrity Design

PCB Geometry present

- A functional design, with all decoupling capacitors already placed on PCB
- PI Engineer may want to:
 - Increase capacitor count in order to make design more robust (i.e. overclocking, etc.)
 - Reduce the capacitor count
 - Reduce number of different capacitor types used
 - Redesign using lower cost capacitors
 - Chose appropriate capacitor location



- Automated PI Optimization : An Automated Approach to investigate into Decoupling Analysis.
- Simulation > Pladvisor...
- A functional design, with all decoupling capacitors already placed on PCB
- PI Engineer may want to:
 - Increase capacitor count in order to make design more robust
 - Reduce the capacitor count
 - Reduce number of different capacitor types used
 - Redesign using lower cost capacitors
 - Chose appropriate capacitor location





Genetic Algorithm Setup Optimized for Impedance Optimized for # of Caps Optimized for Capacitor Types Optimized for Price

ANSYS Automated PI Optimization 5 Easy Steps

1. Define Ports and Impedance Targets



ANSYS[®] **Automated PI Optimization**

5 Easy Steps Select Capacitors for Automated Optimization 2.

1				
Part Name	Ref. Des.	Value (F)	Optimize	^
CAPACITOR_CDR04	C30	1E-07		
CAPACITOR_CDR04	C41	1E-07		
CAPACITOR_CDR04	C58	1E-07		
CAPACITOR_CDR04	C57	1E-07		
CAPACITOR_CDR04	C56	1E-07		
CAPACITOR_CDR04	C55	1E-07		
CAPACITOR_CDR04	C54	1E-07		
CAPACITOR_CDR04	C52	1E-07		
CAPACITOR_CDR04	C50	1E-07		
CAPACITOR_CDR04	C53	1E-07		
CAPACITOR_CDR04	C2	1E-07		
CAPACITOR_CDR04	C49	1E-07		
CAPACITOR_CDR04	C51	1E-07		
CAPACITOR_CDR04	C48	1E-07		
CAPACITOR_CDR04	C37	1E-07		_
CAPACITOR_CDR04	C29	1E-07		
CAPACITOR_CDR04	C17	1E-07		
CAPACITOR_CDR04	C28	1E-07		
CAPACITOR_CDR04	C27	1E-07		
CAPACITOR_CDR04	C39	1E-07		
CAPACITOR_CDR04	C38	1E-07		
CAPACITOR_CDR04	C18	1E-07		
CAPACITOR_CDR04	C14	1E-07		
CAPACITOR_CWR06-10V,47,10%	C10	1E-07		
CAPACITOR_CWR06-10V,47,10%	C9	1E-07		
RLC_XYZ_C	C66	1E-07		
RLC_XYZ_C	C70	1E-07		
RLC_XYZ_C	C71	1E-07		
RLC_XYZ_C	C72	1E-07		
RLC_XYZ_C	C65	1E-07		
RLC_XYZ_C	C67	1E-07		
RLC_XYZ_C	C68	1E-07		
RLC XYZ C	C69	1E-07		~

ANSYS Automated PI Optimization 5 Easy Steps

3. Select Candidate Capacitors for Optimizer

PI Optimizer Wizard Step 3	1										X
Capacitors Selected for Optimization				Imper	lance						_
	18										
Part Name Rer, Des.					\sim						
CAPACITOR_CWR06-10V,47,10% C10						<				1	
CAPACITOR_CWR06-10V,47,10% C9	1E2			~		\searrow				1	
CAPACITOR_CDR04 C2				~			\sim		\times		
CAPACITOR_CDR04 C11		$\langle \rangle$									
CAPACITOR_CDR04 C13											
CAPACITOR_CDR04 C14	E N										
CAPACITOR_CDR04 C15	호 _{1E0}						-		<u> </u>	¥ I	
CAPACITOR_CDR04 C17	5				~		X		\sim	v	
CAPACITOR_CDR04 C18	<u> 1</u>					-1		1			
CAPACITOR_CDR04 C19	1E-1	\sim				X	\wedge	/			
CAPACITOR_CDR04 C20							/				
CAPACITOR_CDR04 C21					-		/				
CAPACITOR_CDR04 C22	1E-2					V	1				
CAPACITOR_CDR04 C23						Ŷ					
CAPACITOR_CDR04 C24	15.2										
CAPACITOR_CDR04 C25	1E-5 1E-4	1E-3	1E-2 1E-1	1	EO	1E1		1E2	1E3	1E4	
CAPACITOR_CDR04 C26				Freque	ncy [MHz]						
CAPACITOR_CDR04 C27											
CAPACITOR_CDR04 C28	Vendor	Series	Part Name	Plot	Candidate	Value (F)	EIA Size	Cost (\$)	SBE (Hz)	S min (dB)	~
CAPACITOR_CDR04 C29	Kemet	T/91C	T491C226M016AT		Add	2.2E-05	2312	0	3 26127E±06	-56 5214	
CAPACITOR_CDR04 C30	Komot	T491C	T491C226M020AT	H	Add	2.20.05	2212	0	2 261276+06	-50.5214	
CAPACITOR_CDR04 C31	Kemet	T491C	T491C220M0204T	H	Add	2.20.05	2012	0	3.20127E+00	-30.3214 E7 770E	_
CAPACITOR_CDR04 C32	Kennet	T401C	T 401 C220M0204T		LLA	2.20-00	2012	0	3.00007E+06	57,0000	_
CAPACITOR_CDR04 C33	Kemet	1431L	T 431C227M006AT		Add	0.00022	2312	0	1.23873E+06	-37.6332	_
CAPACITOR_CDR04 C34	Kemet	1491L	1491C335M025A1		Add	3.3E-06	2312	U	9.19728E+06	-47.2703	_
	Kemet	14910	1491C335M035A1		Add	3.3E-06	2312	0	7.90069E+06	-50.6705	
	Kemet	14910	T491C336M004AT		Add	3.3E-05	2312	U	2.91221E+06	-55.9167	~
	<										>
Assigned Candidate Models	Filters										
Vendor Series Part Name	Vender	Show Series	Show 🔼	FIA	Size Show		Filter	Quantity	Min	Mav	
Kemet T491C T491C105M050AT	AVX	0201		1012				Value (F)	0	0.001	15
Kemet T491C T491C106M010AT	Komot	0201		1012		_		CDE Dongo I	U-1) 0	2.103	2755 +10
Kemet 1491C 1491C10/M004AT	Murata	0402		1825				C min Donge	(dP) .100 911	2.103	224
Kemet T491C T491C155M035AT	Paraca	0402		2220				COD David	(ub) -106.311	-7.37	224
Kemet T491C T491C157M004AT	Panasonic	0008		2225		- 11		ESR Hange	(onms) 4.33788	1.00 0004	86 IF
Kemet T491C T491C225M025AT	Samsung	0603		▶ 2312				ESL Hange (HJ U	1.#IN	41-
Kemet T491C T491C226M010AT	IDK	0612		2816	6			Cost (\$)	U	U	
Kemet T491C T491C227M006AT 🗸	YUDEN	0805		2823	3						
		1206		Othe	er 📃	~					
Remove Plot Z11							_				
								Previous	Next 🔁	Cancel	×
Inc December 7, 2016											

ANSYS How to Determine Candidate Capacitors

- 1. User choice based off of BOM
 - Enter capacitor selections
- 2. User choice based off of filtered selection
- 3. Automated selection using SimplePI



ANSYS Automated PI Optimization 5 Easy Steps

- 4. Setup Optimization Criteria
 - Total Price
 - Total Number of Caps
 - Total Number of Cap Types
 - Total Capacitor Area
 - SYZ Sweep

5. Launch Optimizer and Analyze Results

I P	l Optimizer Wizard Step 4	
	Simulation	
	Name	PI Opt Sim 1
	S-parameter Source	[Recompute]
	Attributes to Minimize	
	🔽 Total price	
	🔽 Total capacitor area	
	Total number of capacitors	
	Total number of capacitor ty	
	Optimizer Control Parameters	
	Members per generation	5
	Number of generations	40
	Cap. attachment probability	.7
	Number of iterations	
	Thresholds	
	Maximum total price (\$)	5.00
	Maximum total capacitor area (4000.00
	Maximum number of capacitors	100
	Maximum number of capacitor t	10
	S-parameter Simulation Optio	ins
	Impedance Mask Range	100Hz -> 1E+09Hz
	Sweep Range	1000Hz -> 1E+09Hz, 301 points
	S-parameter Sweep Configuration	Edit
	Port Reference Impedance	50ohms
	Revious La	unch Optimizer 🛃 🛛 Cancel 💢

ANSYS Optimized Results Without Embedded Capacitance

Time = 15min 7sec

- Frequency Setup
 - 1KHz <= f < 1GHz</p>
 - 50 Points/decade
- Genetic Algorithm Setup
 - Optimized for Impedance
 - Optimized for # of Caps
 - Optimized for Capacitor Types
 - Optimized for Price
 - 100 Members
 - 1000 Iterations

Original solution

- Total # Caps: 74
- Capacitor types:
 - All ideal

Optimized Solution

- Total # Caps: 18
- Capacitor Types = 5
 - AVX, Samsung, and Kemet



ANSYS Loop inductance

After running an optimization in PI advisor right-click the PI Advisor Simulation name in the Results workspace to obtain the loop inductance between each port/capacitor

Provides intuitive plot to analyze capacitor layout thereby minimizing loop inductance


Realize Your Product Promise™



EMI/ EMC simulation Basics

Fluid Dynamics

Structural Mechanics

Electromagnetics

Systems and Multiphysics



First design and optimize PDS

- Low plane impedance
- Minimal resonances

Perform FFT of transient waveforms

- Add current/voltage sources at IC locations
- Measure Near/Far fields in Frequency band of interest

Place PCB/PKG in enclosure model

- Plot fields using HFSS
- Measure effects of shielding



Far/Near-field Calculation

- Explicit field is calculated from SIWave solution
- Far/Near-field Green's function is used to determine fields in all space.







ANSYS Slwave - Far Field Plotting



Add sources to physical location of ICS and specify max current draw or voltage



Emission test plot @ 3m

ANSYS Shielding Analysis

Slwave field solution can be used as a radiation source for HFSS



Dynamically link Slwave to HFSS to plot the field strengths around the enclosure

ANSYS System Analysis (Verification)

Design Setup for System Analysis



ANSYS What is a Full System EMI/EMC Methodology

State of the art EMI/EMC simulation method that

- Utilizes the best in class tools
- Incorporates physical board layouts
- Uses real world transient signals
- Takes into account full 3D enclosures
- Seamlessly combines frequency and time domain simulation tools to predict EMI

What are the tools needed?

- Board analysis > Slwave
- Full 3D enclosure > HFSS
- Realistic clock/timing, and digital signals > AEDT
- CAD links > ALinks

ANSYS What are the steps ?

- 1. Import PCB layout into ALinks or Slwave
- 2. Perform analysis of PCB in Siwave
- 3. Dynamically link SIwave results into ANSYS Electronics Desktop (AEDT) Circuit Design
- 4. Attach drivers and receivers in AEDT to linked SIwave model
- 5. Perform a time/frequency domain analysis of entire system in AEDT
- 6. Push voltage/excitation levels back to SIwave
- 7. Dynamically link the SIwave model into AEDT HFSS Design
- 8. Solve the full system in AEDT HFSS Design



ANSYS The Slwave simulation

1) Layout in eCAD tool is imported into Slwave





1a) Simulation is setup and run

ANSYS° **The AEDT Simulation**

2) Slwave model is dynamically linked into AEDT

2a) Drivers and receivers are added to the circuit and simulated



Ansot LLC

3) Results from AEDT are pushed back into Slwave

3a) Fields near to the PCB are calculated



28 Jan 2009

Ansoft Corporation

XY Plot 1 EMI4Cat ff 20:29:00

Emax_at_3m EMI4Cat_ff

- 4 ×

ANSYS Back to Slwave

ANSYS Linking to HFSS







Siwave_radiation.pdf

Siwave_dynamic_link.pdf

ANSYS Accessing the ANSYS Customer Portal

https://support.ansys.com/portal/site/AnsysCustomerPortal/

Registration and login information can be requested from us

